MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Plastic Medium-Power Complementary Silicon Transistors

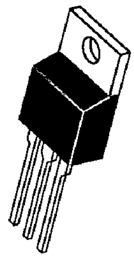
. . . designed for general–purpose amplifier and low–speed switching applications.

- High DC Current Gain —
  h_{FE} = 2500 (Typ) @ I_C = 4.0 Adc
- Collector Emitter Sustaining Voltage — @ 100 mAdc
  $V_{CEO(sus)}$ = 80 Vdc (Min) — BDX53B, 54B
  = 100 Vdc (Min) — BDX53C, 54C
- Low Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C = 3.0 Adc
  = 4.0 Vdc (Max) @ I_C = 5.0 Adc
- Monolithic Construction with Built–In Base–Emitter Shunt Resistors
- TO–220AB Compact Package

NPN
BDX53B
BDX53C*
PNP
BDX54B
BDX54C*

*Motorola Preferred Device

DARLINGTON
8 AMPERE
COMPLEMENTARY
SILICON
POWER TRANSISTORS
80–100 VOLTS
65 WATTS



CASE 221A–06
TO–220AB

MAXIMUM RATINGS

Rating	Symbol	BDX53B BDX54B	BDX53C BDX54C	Unit
Collector–Emitter Voltage	V_{CEO}	80	100	Vdc
Collector–Base Voltage	V_{CB}	80	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0		Vdc
Collector Current — Continuous Peak	I_C	8.0 12		Adc
Base Current	I_B	0.2		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	60 0.48		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	70	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	70	°C/W

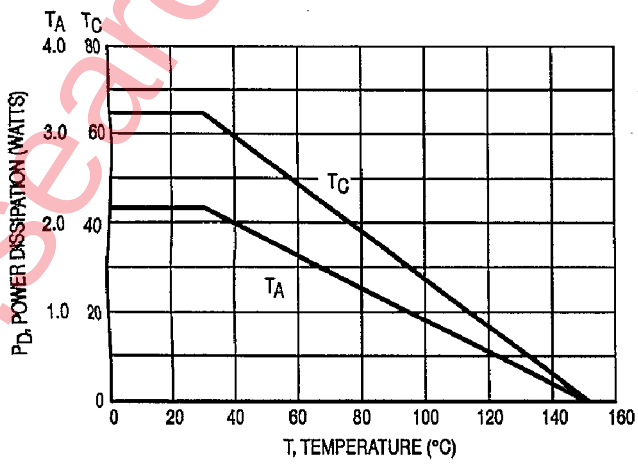


Figure 1. Power Derating

REV 7

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Sustaining Voltage (1) (I_C = 100 mAdc, I_B = 0)	BDX53B, BDX54B BDX53C, BDX54C	$V_{CEO(sus)}$	80 100	— —	Vdc
Collector Cutoff Current (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	BDX53B, BDX54B BDX53C, BDX54C	I_{CEO}	— —	0.5 0.5	mAdc
Collector Cutoff Current (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	BDX53B, BDX54B BDX53C, BDX54C	I_{CBO}	— —	0.2 0.2	mAdc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)		h_{FE}	750	—	—
Collector–Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 12 mAdc)		$V_{CE(sat)}$	— —	2.0 4.0	Vdc
Base–Emitter Saturation Voltage (I_C = 3.0 Adc, I_C = 12 mA)		$V_{BE(sat)}$	—	2.5	Vdc
DYNAMIC CHARACTERISTICS					
Small–Signal Current Gain (I_C = 3.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)		h_{fe}	4.0	—	—
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	BDX53B, 53C BDX54B, 54C	C_{ob}	— —	300 200	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

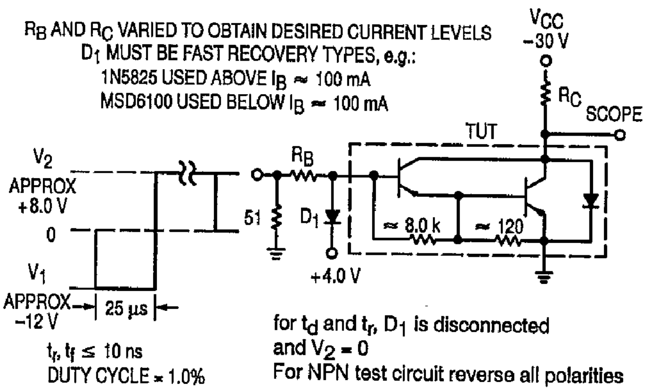


Figure 2. Switching Time Test Circuit

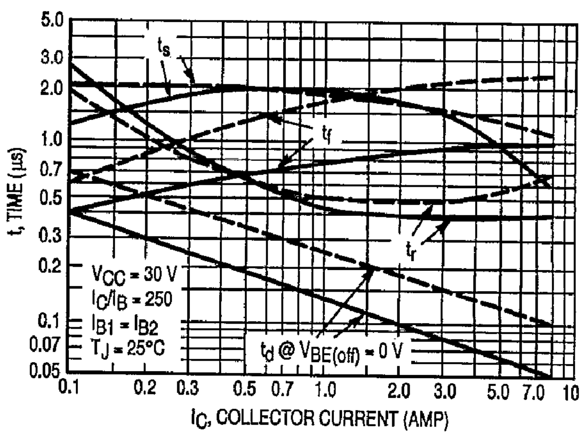


Figure 3. Switching Times

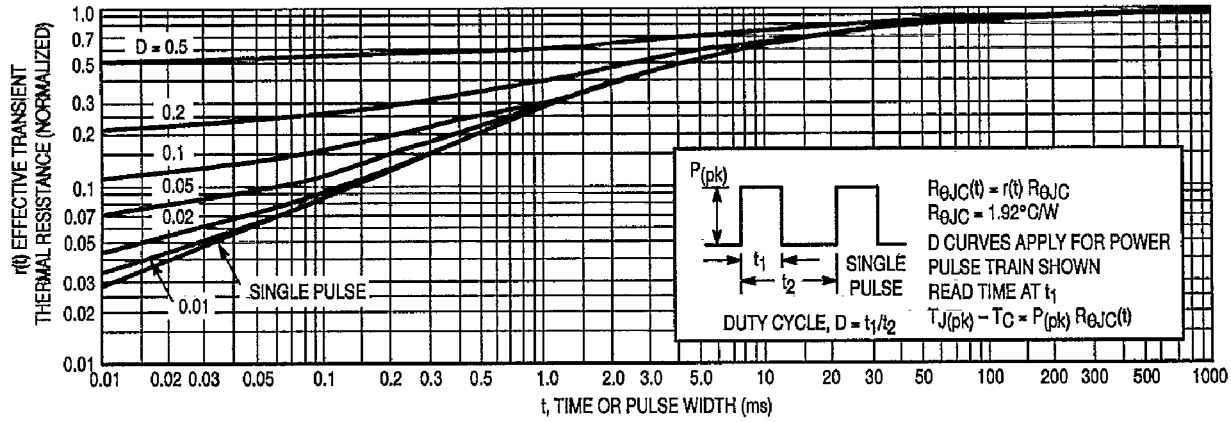


Figure 4. Thermal Response

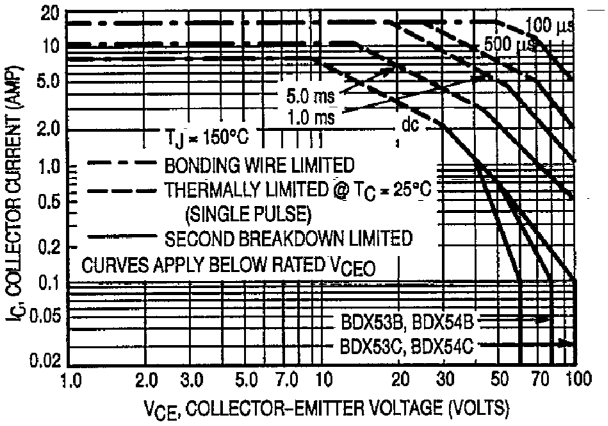


Figure 5. Active–Region Safe Operating Area

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

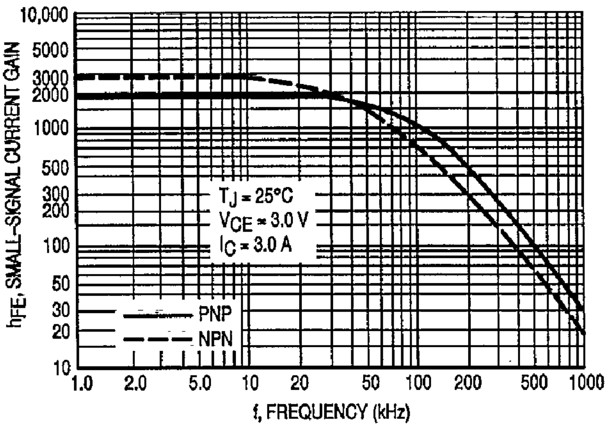


Figure 6. Small-Signal Current Gain

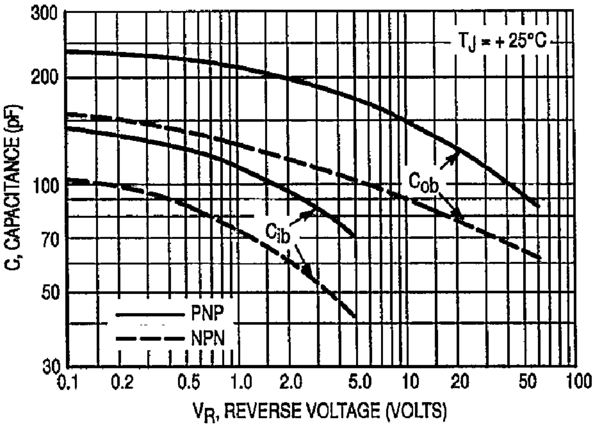


Figure 7. Capacitance

NPN
BDX53B, 53C

PNP
BDX54B, 54C

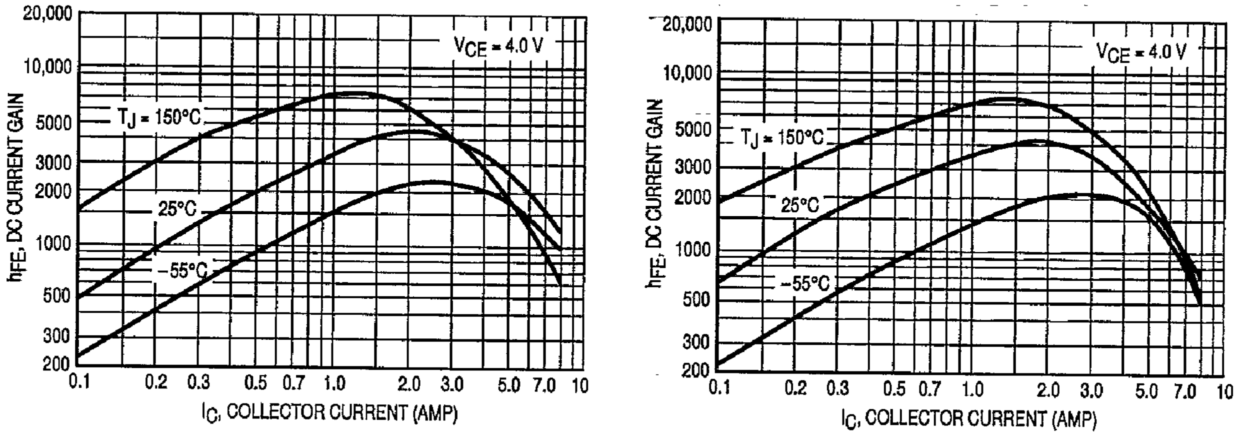


Figure 8. DC Current Gain

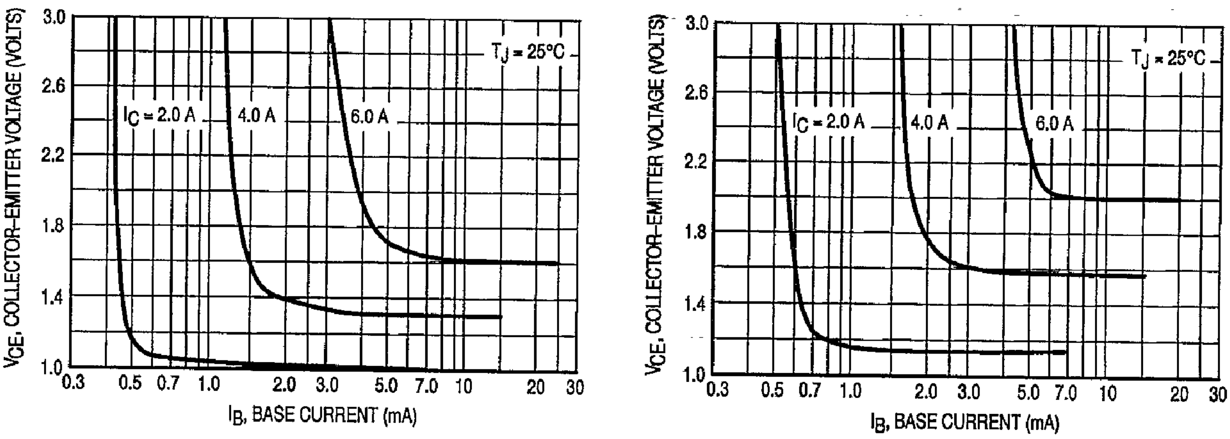


Figure 9. Collector Saturation Region

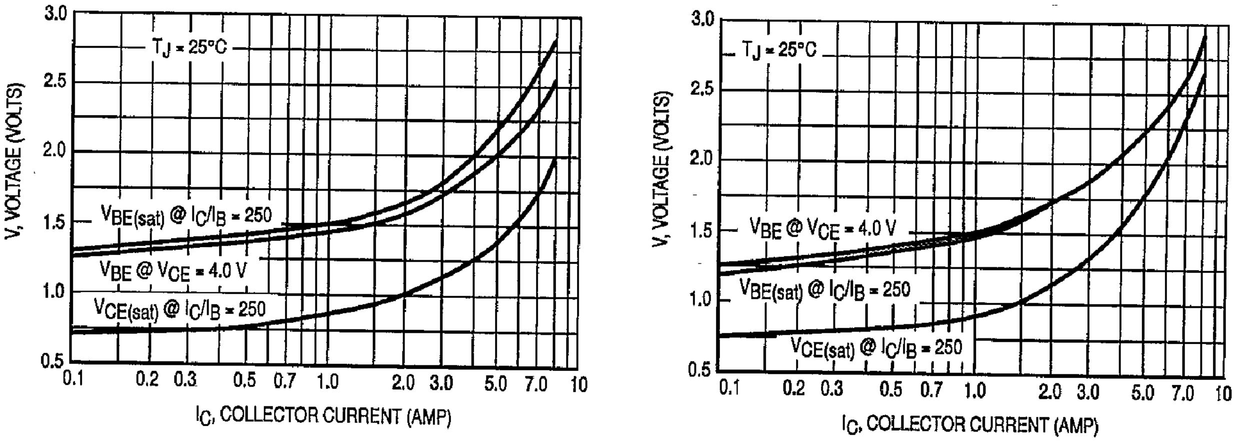


Figure 10. "On" Voltages

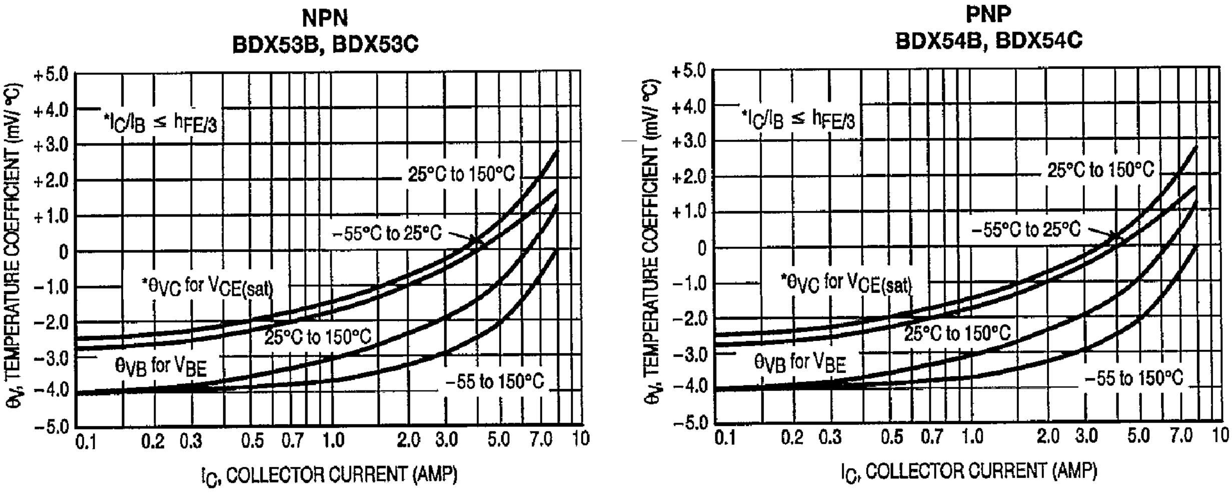


Figure 11. Temperature Coefficients

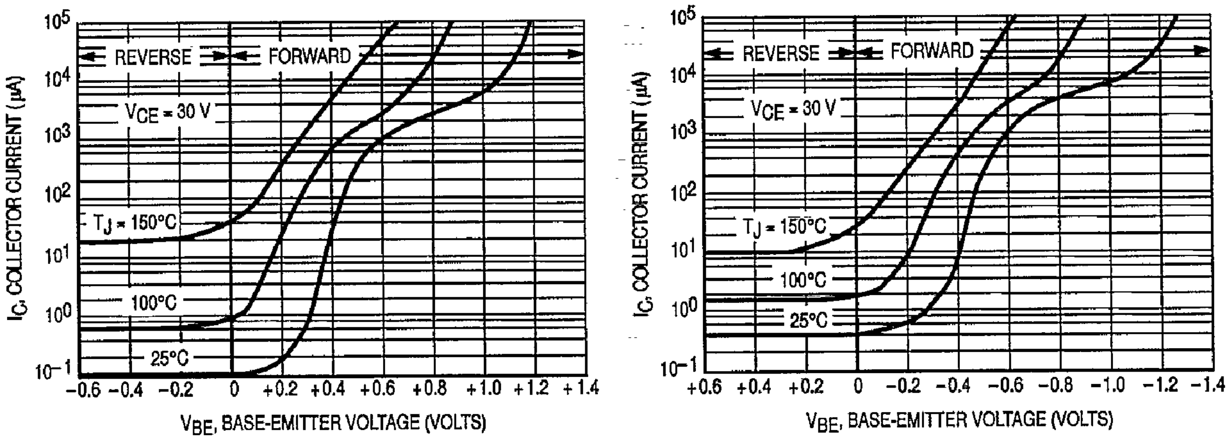


Figure 12. Collector Cut–Off Region

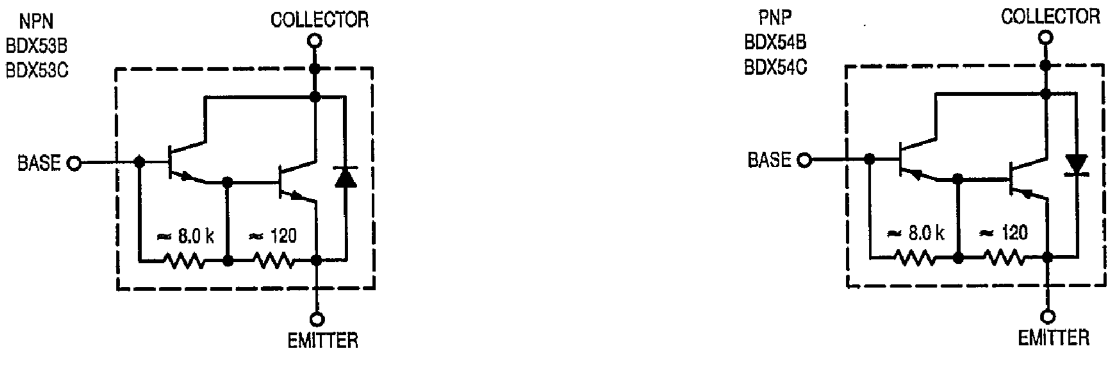


Figure 13. Darlington Schematic