- 3-State Outputs Drive Bus Lines Directly
- Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs


## description

These octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the $B$ bus or from the $B$ bus to the $A$ bus depending upon the logic level at the direction-control (DIR) input. The output enable $(\overline{\mathrm{OE}})$ input can be used to disable the device so the buses are effectively isolated.

The SN74F245 is available in Tl's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.
The SN54F245 is characterized for operation over the full military temperature range of $-55^{\circ} \mathrm{C}$ to $125^{\circ} \mathrm{C}$. The SN74F245 is characterized for operation from $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$.

SN54F245 . . J PACKAGE
SN74F245 . . . DB, DW, OR N PACKAGE
(TOP VIEW)

| DIR ${ }_{1}$ | $\mathrm{V}_{20} \mathrm{~V} \mathrm{VCC}$ |
| :---: | :---: |
| A1 2 | ${ }_{19}{ }^{\text {OE }}$ |
| A2 ${ }^{\text {a }}$ | 18 B1 |
| A3 [4 | 17 B2 |
| A4 5 | 16 B3 |
| A5 [6 | 15 B4 |
| A6 [7 | 14 B5 |
| A7 [8 | $13]$ B6 |
| A8 [9 | $12]$ B7 |
| GND [10 | 11] B8 |

SN54F245 ... FK PACKAGE (TOP VIEW)


FUNCTION TABLE

| INPUTS |  | OPERATION |
| :---: | :---: | :---: |
| $\overline{\mathrm{OE}}$ | DIR |  |
| L | L | B data to $A$ bus |
| L | $H$ | A data to $B$ bus |
| $H$ | $X$ | Isolation |

## logic symbol $\dagger$


$\dagger$ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



To Seven Other Channels
absolute maximum ratings over operating free-air temperature range (unless otherwise noted) $\ddagger$

$\ddagger$ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

## recommended operating conditions

|  |  |  |  | 54F2 |  |  | N74F24 |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | MIN | NOM | MAX | MIN | NOM | MAX | UNT |
| $\mathrm{V}_{\text {CC }}$ | Supply voltage |  | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| $\mathrm{V}_{\mathrm{IH}}$ | High-level input voltage |  | 2 |  |  | 2 |  |  | V |
| $\mathrm{V}_{\text {IL }}$ | Low-level input voltage |  |  |  | 0.8 |  |  | 0.8 | V |
| IIK | Input clamp current |  |  |  | -18 |  |  | -18 | mA |
|  | High-level output current | A1 thru A8 |  |  | -3 |  |  | -3 | mA |
| Ion | High-levelouput current | B1 thru B8 |  |  | -12 |  |  | -15 |  |
| OL | Low-level output current | A1 thru A8 |  |  | 20 |  |  | 24 | mA |
| OL | Low-leveloutput curent | B1 thru B8 |  |  | 48 |  |  | 64 |  |
| $\mathrm{T}_{\text {A }}$ | Operating free-air temperature |  | -55 |  | 125 | 0 |  | 70 | ${ }^{\circ} \mathrm{C}$ |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER |  | TEST CONDITIONS |  | SN54F245 |  |  | SN74F245 |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | MIN | TYPt | MAX | MIN | TYP† | MAX |  |
| $\mathrm{V}_{\text {IK }}$ |  |  |  | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$, | $\boldsymbol{I}=-18 \mathrm{~mA}$ |  |  | -1.2 |  |  | -1.2 | V |
| $\mathrm{V}_{\mathrm{OH}}$ | A1 thru A8 | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$ | $\mathrm{IOH}^{\prime}=-1 \mathrm{~mA}$ | 2.5 | 3.4 |  | 2.5 | 3.4 |  | V |
|  |  |  | $\mathrm{OH}=-3 \mathrm{~mA}$ | 2.4 | 3.3 |  | 2.4 | 3.3 |  |  |
|  | B1 thru B8 | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$ | $\mathrm{IOH}=-12 \mathrm{~mA}$ | 2 | 3.2 |  |  |  |  |  |
|  |  |  | $\mathrm{IOH}=-15 \mathrm{~mA}$ |  |  |  | 2 | 3.1 |  |  |
|  | Any output | $\mathrm{V}_{\mathrm{CC}}=4.75 \mathrm{~V}$, | $\mathrm{IOH}=-1 \mathrm{~mA}$ to -3 mA |  |  |  | 2.7 |  |  |  |
| VOL | A1 thru A8 | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$ | $\mathrm{IOL}=20 \mathrm{~mA}$ |  | 0.3 | 0.5 |  |  |  | V |
|  |  |  | $\mathrm{IOL}=24 \mathrm{~mA}$ |  |  |  |  | 0.35 | 0.5 |  |
|  | B1 thru B8 | $\mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}$ | $\mathrm{IOL}=48 \mathrm{~mA}$ |  | 0.38 | 0.55 |  |  |  |  |
|  |  |  | $\mathrm{IOL}=64 \mathrm{~mA}$ |  |  |  |  | 0.42 | 0.55 |  |
| 1 | $A$ and $B$ | $V_{C C}=5.5 \mathrm{~V}$ | $\mathrm{V}_{\mathrm{I}}=5.5 \mathrm{~V}$ |  |  | 1 |  |  | 1 | mA |
|  | DIR, $\overline{O E}$ |  | $\mathrm{V}_{\mathrm{I}}=7 \mathrm{~V}$ |  |  | 0.1 |  |  | 0.1 |  |
|  | A and B | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, | $\mathrm{V}_{\mathrm{I}}=2.7 \mathrm{~V}$ |  |  | 70 |  |  | 70 | $\mu \mathrm{A}$ |
| ${ }^{1 \mathrm{IH}^{+}}$ | DIR, $\overline{O E}$ |  |  |  |  | 20 |  |  | 20 |  |
|  | $A$ and $B$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, | $\mathrm{V}_{\mathrm{I}}=0.5 \mathrm{~V}$ |  |  | -0.65 |  |  | -0.65 | mA |
| ${ }_{1 L}{ }^{+}$ | DIR, $\overline{O E}$ |  |  |  |  | -1.2 |  |  | -1.2 |  |
| S | A1 thru A8 | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$, | $\mathrm{V}_{\mathrm{O}}=0$ | -60 |  | -150 | -60 |  | -150 | mA |
| Ios | B1 thru B8 |  |  | -100 |  | -225 | -100 |  | -225 |  |
| ICC |  | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}$ | Outputs high |  | 70 | 90 |  | 70 | 90 | mA |
|  |  | Outputs low |  | 95 | 120 |  | 95 | 120 |  |
|  |  | Outputs disabled |  | 85 | 110 |  | 85 | 110 |  |

$\dagger$ All typical values are at $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$.
$\ddagger$ For I/O ports, the parameters $\mathrm{I}_{\mathrm{IH}}$ and $\mathrm{I}_{\mathrm{IL}}$ include the off-state output current.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

## switching characteristics (see Note 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}, \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \\ & \mathrm{R}_{\mathrm{L}}=500 \Omega, \\ & \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \end{aligned}$ |  |  | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V}, \\ & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF}, \\ & \mathrm{R}_{\mathrm{L}}=500 \Omega, \\ & \mathrm{~T}_{\mathrm{A}}=\operatorname{MIN} \text { to MAX } \dagger \end{aligned}$ |  |  |  | UNIT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | F245 |  | SN5 | 245 | SN74 | 245 |  |
|  |  |  | MIN | TYP | MAX | MIN | MAX | MIN | MAX |  |
| tPLH | A or B | B or A | 1.7 | 3.8 | 6 | 1.2 | 7.5 | 1.7 | 7 | ns |
| tPHL |  |  | 1.7 | 4.2 | 6 | 1.2 | 7.5 | 1.7 | 7 |  |
| tPZH | $\overline{\mathrm{OE}}$ | A or B | 2.2 | 4.9 | 7 | 1.7 | 9 | 2.2 | 8 | ns |
| tPZL |  |  | 2.7 | 5.6 | 8 | 2.2 | 10 | 2.7 | 9 |  |
| tPHZ | $\overline{\mathrm{OE}}$ | A or B | 2.2 | 4.6 | 6.5 | 1.7 | 9 | 2.2 | 7.5 | ns |
| tplZ |  |  | 1.2 | 4.6 | 6.5 | 1.2 | 10 | 1.2 | 7.5 |  |

[^0]
## PACKAGING INFORMATION

| Orderable Device | Status <br> (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <br> (2) | Lead/Ball Finish <br> (6) | MSL Peak Temp <br> (3) | Op Temp ( ${ }^{\circ} \mathrm{C}$ ) | Device Marking <br> (4/5) | Samples |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 85511012A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N/A for Pkg Type | -55 to 125 | $\begin{aligned} & 85511012 A \\ & \text { SNJ54F } \\ & \text { 245FK } \end{aligned}$ | Samples |
| 8551101RA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | $\begin{aligned} & \text { 8551101RA } \\ & \text { SNJ54F245J } \end{aligned}$ | Samples |
| 8551101SA | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8551101SA <br> SNJ54F245W | Samples |
| JM38510/34803B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | $\begin{aligned} & \text { JM38510/ } \\ & \text { 34803B2A } \end{aligned}$ | Samples |
| JM38510/34803BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N/ A for Pkg Type | -55 to 125 | $\begin{aligned} & \text { JM38510/ } \\ & \text { 34803BRA } \end{aligned}$ | Samples |
| JM38510/34803BSA | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | $\begin{aligned} & \text { JM38510/ } \\ & \text { 34803BSA } \end{aligned}$ | Samples |
| M38510/34803B2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | $\begin{aligned} & \text { JM38510/ } \\ & \text { 34803B2A } \end{aligned}$ | Samples |
| M38510/34803BRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | $\begin{aligned} & \text { JM38510/ } \\ & \text { 34803BRA } \end{aligned}$ | Samples |
| M38510/34803BSA | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | $\begin{aligned} & \text { JM38510/ } \\ & \text { 34803BSA } \end{aligned}$ | Samples |
| SN54F245J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N/ A for Pkg Type | -55 to 125 | SN54F245J | Samples |
| SN74F245DBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS \& no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | F245 | Samples |
| SN74F245DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS \& no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | F245 | Samples |
| SN74F245DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS \& no $\mathrm{Sb} / \mathrm{Br}$ ) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | F245 | Samples |
| SN74F245N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free <br> (RoHS) | CU NIPDAU | N/A for Pkg Type | 0 to 70 | SN74F245N | Samples |
| SN74F245NE4 | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN74F245N | Samples |
| SN74F245NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS \& no $\mathrm{Sb} / \mathrm{Br}$ ) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 74F245 | Samples |
| SNJ54F245FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | $85511012 A$ <br> SNJ54F | Samples |


| Orderable Device | Status <br> (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <br> (2) | Lead/Ball Finish <br> (6) | MSL Peak Temp <br> (3) | Op Temp ( ${ }^{\circ} \mathrm{C}$ ) | Device Marking (4/5) | Samples |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  |  |  |  |  | 245FK |  |
| SNJ54F245J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | $\begin{aligned} & \text { 8551101RA } \\ & \text { SNJ54F245J } \end{aligned}$ | Samples |
| SNJ54F245W | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 8551101SA SNJ54F245W | Samples |

${ }^{(1)}$ The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
${ }^{(2)}$ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed $0.1 \%$ by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the $<=1000 \mathrm{ppm}$ threshold requirement.
${ }^{(3)}$ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
${ }^{(4)}$ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
${ }^{(5)}$ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
${ }^{(6)}$ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## OTHER QUALIFIED VERSIONS OF SN54F245, SN74F245

- Catalog: SN74F245
- Military: SN54F245

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications


## TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package <br> Type | Package <br> Drawing | Pins | SPQ | Reel <br> Diameter <br> $(\mathbf{m m})$ | Reel <br> Width <br> W1 $(\mathbf{m m})$ | A0 <br> $(\mathbf{m m})$ | B0 <br> $(\mathbf{m m})$ | K0 <br> $(\mathbf{m m})$ | P1 <br> $(\mathbf{m m})$ | W <br> $(\mathbf{m m})$ | Pin1 <br> Quadrant |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SN74F245DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74F245DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74F245NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SN74F245DBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74F245DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74F245NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |

W (R-GDFP-F20)


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)
LEADLESS CERAMIC CHIP CARRIER 28 TERMINAL SHOWN


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS-004

NS (R-PDSO-G**)
14-PINS SHOWN


| DIM PINS ** | 14 | 16 | 20 | 24 |
| :---: | :---: | :---: | :---: | :---: |
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.


| DIM PINS ** | 14 | 16 | 18 | 20 |
| :---: | :---: | :---: | :---: | :---: |
| A | 0.300 <br> $(7,62)$ <br> BSC | 0.300 <br> $(7,62)$ <br> BSC | 0.300 <br> $(7,62)$ <br> BSC | 0.300 <br> $(7,62)$ <br> BSC |
| B MAX | 0.785 <br> $(19,94)$ | .840 <br> $(21,34)$ | 0.960 <br> $(24,38)$ | 1.060 <br> $(26,92)$ |
| B MIN | - | - | - | - |
| C MAX | 0.300 <br> $(7,62)$ | 0.300 <br> $(7,62)$ | 0.310 <br> $(7,87)$ | 0.300 <br> $(7,62)$ |
| C MIN | 0.245 <br> $(6,22)$ | 0.245 <br> $(6,22)$ | 0.220 <br> $(5,59)$ | 0.245 <br> $(6,22)$ |



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.


| DIM PINS ** | $\mathbf{1 4}$ | $\mathbf{1 6}$ | $\mathbf{2 0}$ | $\mathbf{2 4}$ | $\mathbf{2 8}$ | $\mathbf{3 0}$ | $\mathbf{3 8}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

N (R-PDIP-T**)
PLASTIC DUAL-IN-LINE PACKAGE
16 PINS SHOWN


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D The 20 pin end lead shoulder width is a vendor option, either half or full width.


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side
5. Reference JEDEC registration MS-013.


NOTES: (continued)
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.


SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

SCALE:6X

NOTES: (continued)
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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[^0]:    $\dagger$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 2: Load circuits and waveforms are shown in Section 1.

