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## Introduction

## PRISMP

The PRISM1KIT-EVAL wireless LAN PC card is a complete wireless high speed modem utilizing the Intersil PRISM® Direct Sequence Spread Spectrum (DSSS) wireless transceiver chip set. The card is packaged in an open frame PCMCIA Type II extended coverset for evaluation access and a connector output for use in the laboratory. Evaluation kits include two cards, Microsoft ${ }^{(8)}$ Windows® 95 software and documentation to get your WLAN evaluation started quickly. The PRISM1KIT-EVAL is not FCC approved as an intentional radiator and is intended for use with cabled connections only (30dB antenna port to antenna port attenuation recommended). An FCC experimental license is required while transmitting over the air with unapproved equipment. Please refer to the WLANKITPR1-KIT for an FCC-approved radio kit for wireless LAN evaluations. This application note details the RF and analog design of these cards. The physical layer (PHY) sections of these PC Cards are described in detail. The medium access control (MAC) section of the PC Cards will be described in detail in the pending AMD application note titled "Wireless LAN DSSS PC Card Reference Design" [1].

Figure 1 shows a block diagram of the reference radio design. This radio has been designed to conform to the draft IEEE 802.11 specification but does not include the antenna diversity selection.

The specifications of the PC Card Wireless LAN are as follows:

## Ordering Information

| PART NUMBER | DESCRIPTION | CARDS PER KIT |
| :--- | :--- | :---: |
| PRISM1KIT-EVAL | Evaluation Kit | 2 |

## General Specifications

- Targeted Standard . . . . . . . . . . . . . . . IEEE 802.11 (Draft)
- Data Rate . . . . . . . . . . . . . . . . . . . . . . . . . . 1Mbps DBPSK 2Mbps DQPSK
- Range . . . . . . . . . . . . . . . . . . 400 ft Indoor (Typ) (Note 1) 3700ft Outdoor (Typ) (Note 1)
- Frequency Range . . . . . . . . . . . . . . 2412 MHz to 2484 MHz
- Step Size . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1MHz
- IF Frequency . . . . . . . . . . . . . . . . . . . . . . . . . . . . 280MHz
- IF Bandwidth. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 17MHz
- RX/TX Switching Speed . . . . . . . . . . . . . . . . . . . $2 \mu \mathrm{~s}$ (Typ)
- Operating Voltage. . . . . . . . . . . . . . . . . 4.5 $\mathrm{V}_{\mathrm{DC}}-5.5 \mathrm{~V}_{\mathrm{DC}}$



## Receive Specifications

- Sensitivity . . . . -91dBm (Typ), 1Mbps, 8E-2 FER (Note 3) -88 dBm (Typ), 2Mbps, 8E-2 FER (Note 3)
- Input Third Order Intercept Point
-20dBm (Typ)
- Image Rejection 65dB (Typ)
- IF Rejection 80dB (Typ)
- Adjacent Channel Rejection. . . . . . . . . . . . . . . 63dB (Typ) at 25 MHz Offset
Supply Current . . . 287mA (Typ), 2Mbps, 100\% Duty Cycle


## Transmit Specifications

- Output Power . . . . . . . . . . . . . . . . . . . . . . +17.5dBm (Typ)
- Transmit Spectral Mask . . .-32dBc (Typ) at First Side-Lobe
- Supply Current . . . . 488mA (Typ), 2Mbps, 100\% Duty Cycle NOTES:

1. Using M/A-COM AND-C-107 omnidirectional antenna.
2. AM 79 C 930 limited to $0^{\circ} \mathrm{C}$ to $70^{\circ} \mathrm{C}$.
3. $\mathrm{FER}=$ Frame Error Rate or Packet Error Rate.
4. Recovery times do not include MAC recovery.

## Receive Processing

Referring to the block diagram in Figure 1, the schematic on our web site [2], and the bill of materials in Appendix A, a single antenna is used. Up to two antennas are supported in the HFA3824A [3] Baseband Processor to implement diversity, countering the adverse effects of multipath fading. As space is at a premium in a PC Card environment, only one antenna is used. In an actual system implementation, if one can achieve diversity in at least one end of a link, such as at the access point where it is possible to achieve physical separation between diversity antennas, multipath performance will be improved.


From the antenna, the received input is applied to FL3 and FL6, a Toko TDF2A-2450T-10 two pole dielectric bandpass filters, which are used to provide image rejection for the receiver. The IF frequency is 280 MHz , and low-side injection is used, thereby placing the received image 560 MHz below the tuned channel. FL3 and FL6 also provide protection for the RF front-end from out of band interfering signals.
The T/R switch is integrated in the HFA3925 [4] RF Power Amplifier (RFPA). The HFA3925 RFPA operates from the unregulated 5V PC Card supply.

Following the T/R switch, the HFA3424 [5] Low Noise Amplifier (LNA) is used to set the receiver noise figure. The HFA3424 LNA operates from a regulated 3.5 V supply. A logic-level PMOS switch, RF1K49093 [9], is used to control the drain supply voltage to the HFA3424 LNA, and implement a power down mode when transmitting.

A trade-off between noise figure and input intercept point exists in any receiver, to balance these conflicting requirements in the PRISM radio, an attenuator follows the HFA3424 LNA, and it may be mounted. To improve input intercept point, this attenuation may be increased. The cascaded front-end noise figure, input intercept point, and gain distribution analysis are shown in Table 1.

Next, the signal enters the HFA3624 [6] RF/IF Converter LNA section, which aids in setting receiver NF. FL1 is used to suppress image noise generated in both the HFA3424 LNA and the HFA3624 LNA, and is a Murata LFJ3003B2442B084 two pole monolithic LC bandpass filter. Only modest attenuation at the image frequency is required. The insertion loss is not critical, since at this point in the receiver, component loss or NF is offset by the preceding gain stages. All sections of the HFA3624 RF/IF Converter operate from a regulated 3.5 V supply.
Down-conversion from the $2.4 \mathrm{GHz}-2.5 \mathrm{GHz}$ band is performed in the HFA3624 RF/IF Converter mixer section. As previously mentioned, the IF center frequency is 280 MHz , and low-side local oscillator (LO) injection is used. A discrete LC matching network is used at the mixer output to differentially combine the

IF outputs, as well as match impedance to a $50 \Omega$ environment. A trimmer capacitor is used as part of the narrow-band matching network. An alternative, broadband matching network is described in the HFA3624 RF/IF Converter application note, and does not require any tunable elements. A direct impedance match to the IF filter, U7 could be implemented if desired. The $50 \Omega$ environment was chosen to allow ease in measurement of portions of the radio with external test equipment. An analysis of the mixer spurious responses is shown in Appendix $B$. There are no crossing spurious responses, therefore only tuned responses are shown.

The IF receive filter, U7, is a Toyocom TQS-432 SAW bandpass filter. The center frequency is 280 MHz , the 3 dB bandwidth is 17 MHz , and the differential group delay is less than 100 ns . Insertion loss is typically 6 dB , making it ideal for single-conversion systems. The impedance of the SAW is $270 \Omega$, in parallel with 5 pF , and a series 33 nH inductor is used to match the filter input to $50 \Omega$. The SAW output is matched directly to the IF input of the HFA3724 Quadrature IF Modulator/Demodulator, using a shunt 33nH inductor and $261 \Omega$ resistor. This presents a $250 \Omega$ source impedance to the limiter input, thereby optimizing the limiter's NF. Measured performance of the SAW filter is shown in Appendix C.

In the receive mode, the HFA3724 Quadrature IF Modulator/Demodulator provides two limiting amplifiers, a quadrature baseband demodulator, and two baseband low pass filters. All sections of the HFA3724 operate from a regulated 3.5 V supply. The first limiting amplifier establishes the NF of the IF strip at approximately 7dB. A discrete one pole LC differential filter is placed between the two limiters to restrict the noise bandwidth of the first limiter. As both limiters exhibit a broadband response, with over 400 MHz bandwidth, a noise bandwidth reduction filter is appropriate to ensure that the second limiter is fully limiting on the frontend noise within the signal bandwidth, as opposed to the broadband noise generated by the first limiter. This filter has a center frequency of 280 MHz , and a 3 dB bandwidth of 50 MHz . It consists of a fixed 10 nH inductor and a fixed 20 pF capacitor, as described in the HFA3724 data sheet.

TABLE 1. PRISM CASCADED FRONT-END ANALYSIS

| STAGE | G | GC | F | FC | IP30 | IP30C | IP3IC |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| FL6 RF Filter | -2.0 | -2.0 | 2.0 | 2.0 | 100.0 | 100.0 | 102.0 |
| FL3 RF Filter | -2.0 | -4.0 | 2.0 | 4.0 | 100.0 | 95.9 | 99.9 |
| HFA3925 T/R Switch | -1.2 | -5.2 | 1.2 | 5.2 | 34.0 | 34.0 | 39.2 |
| HFA3424 LNA | 13.0 | 7.8 | 2.0 | 7.2 | 11.1 | 11.0 | 3.3 |
| HFA3624 LNA | 15.6 | 23.4 | 3.8 | 7.4 | 15.0 | 14.7 | -8.7 |
| FL1 RF Filter | -3.0 | 20.4 | 3.0 | 7.4 | 100.0 | 11.7 | -8.7 |
| HFA3624 Mixer | 3.0 | 23.4 | 12.0 | 7.5 | 4.0 | 3.6 | -19.8 |
| U7 IF Filter | -10.0 | 13.4 | 10.0 | 7.5 | 100.0 | -6.4 | -19.8 |
| HFA3724 [7] IF Strip | 0.0 | 13.4 | 7.0 | 7.7 | 100.0 | -6.4 | -19.8 |

Cascaded Gain = 13.4dB Cascaded $\mathrm{NF}=7.7 \mathrm{~dB} \quad$ Cascaded Input IP3 $=-19.8 \mathrm{dBm}$
NOTE: G (individual stage gain, dB), GC (cumulative gain, dB), F (NF, dB), FC (cumulative NF, dB), IP3O (individual stage output IP3, dBm), IP3OC (cumulative output IP3, dBm), IP3IC (cumulative input IP3, dBm).

The gain distribution/limiter noise analysis is shown in Appendix F. If the alternative HFA3624 broadband matching network is used, the HFA3624 mixer conversion gain will be higher, which will help ensure that the second limiter is fully limited on front-end noise.

At the output of the limiters, a $200 \mathrm{mV} \mathrm{V}_{\mathrm{P}-\mathrm{P}}$ differential signal level is maintained under all input conditions. This limited signal is then mixed in quadrature to baseband in the HFA3724 Quadrature IF Modulator/Demodulator. The LO needed for the quadrature mixing is applied at twice the IF frequency, or 560 MHz . A divide by two circuit then provides an accurate quadrature LO for the mixers. The baseband outputs of the quadrature mixers are AC coupled off-chip to the integrated fifth order Butterworth filters. The output levels of the low pass filters are nominally 500 mV P-p single-ended, and are intended to be AC coupled to the HFA3824A Baseband Processor. The AC coupling time constant is approximately 25 times longer than the symbol period, and is implemented with $0.01 \mu \mathrm{~F}$ series capacitors. These coupling capacitors must be taken into account, however, when estimating the time it takes to power up or awaken from sleep mode.

At the input to the HFA3824A Baseband Processor, the quadrature signals are analog to digital converted in wideband 3 bit converters. The sample rate is 22MSPS, which results in two samples per chip. A 22MHz Fox F4106 crystal oscillator is used to provide the main clock for the HFA3824A. The signals are spread spectrum with no DC term, so it is feasible to AC couple the signals to the ADCs and avoid DC bias offsets. The signal at this point has been limited to a constant IF amplitude and then passed through two separate mixer and low pass filter paths. The component variations in these two paths can introduce offsets in amplitude and phase and can also use up some of the headroom in the ADCs. The maximum amplitude variation is 2 dB and the maximum phase balance variation is 4 degrees. Since the signal is limited, the IF signals will have low peak to average ratios even with noise as an input. The I and Q signals will have sinusoidal properties with PSK modulation imposed. It is their combined vector magnitude that is limited, not their individual amplitudes. To optimize the demodulator's performance, the ADCs are operated at the point where they are at full scale on either I or Q one third of the time. To maintain this operating point in the face of component variations, there is an optional active adjustment of the ADC reference voltage by feedback. This avoids the necessity of allowing extra headroom for the variation. The adjustment circuit is very slow and averages the energy from the two channels over both packet and noise conditions.

The HFA3824A Baseband Processor correlates the PN spreading to remove it and to uncover the differential BPSK or QPSK data. The processor initially uses differential detection to identify and lock onto the signal. It then makes measurements of the carrier and symbol timing phase and frequency and uses these to initialize tracking loops for fast
acquisition. Once demodulating and tracking, the processor uses coherent demodulation for best performance. Since this radio uses a spread spectrum signal with 10.4 dB of processing gain $(10 \log 11)$, the signal to noise ratio $(S N R)$ in the chip rate bandwidth is approximately 0 dB when the demodulator is at the desired bit error rate in BPSK. The radio operates with about 2.5 dB of implementation loss relative to theoretical performance and achieves a sensitivity of -91 dBm in the BPSK mode of operation.

The HFA3824A Baseband Processor provides differential decoding and descrambling of the data to prepare it for the Media Access Controller (MAC). The MAC is an AMD AM79C930 PCnet - Mobile controller. All packet signals have a preamble followed by a header containing a start frame delimiter (SFD), other signal related data and a cyclic redundancy check (CRC). The MAC processes the header data to locate the SFD, determine the mode and length of the incoming message and to check the CRC. The MAC then processes the packet data and sends it on through the PC Card interface to the host computer. The MAC checks the packet data CRC to determine the data purity. If corrupted data is received, a retransmission is requested by the MAC which handles the physical layer link protocols.

## Transmit Processing

Data from the host computer is sent to the MAC via the PC Card interface. Prior to any communications, however, the MAC sends a Request to Send (RTS) packet to the other end of the link and receives a Clear to Send (CTS) packet. The MAC then formats the payload data packet (MPDU) by appending it to a preamble and header and sends it on to the HFA3824A Baseband Processor which clocks it in. The HFA3824A Baseband Processor scrambles the packet and differentially encodes it before applying the spread spectrum modulation. The data can be either DBPSK or DQPSK modulated at 1MSPS and is a baseband quadrature signal with I and Q components. The BPSK spreading is an 11 chip Barker sequence that is clocked at 11 MHz and is modulated with the I and Q data components. These are then output to the HFA3724 as CMOS logic signals. Following the RTS/CTS/MPDU is an acknowledge (ACK) packet by the receiving side of the link.

Transmit quadrature single-bit digital inputs are applied to the HFA3724 Quadrature IF Modulator/Demodulator from the HFA3824A Baseband Processor. These inputs are attenuated by $1 / 7$ and DC coupled to the fifth order Butterworth low pass filters, which are used to provide shaping of the phase shift keyed (PSK) signal. The required transmit spectral mask, at the antenna, is -30 dBc at the first side-lobe relative to the mainlobe. An unfiltered PSK waveform would have the first side-lobe suppressed only -13 dBc . The fifth-order filters are tuned to an approximate 7.7 MHz cutoff, using a $909 \Omega$ fixed tuning resistor external to the HFA3724.

In the PC Card wireless LAN, the goal is to control the regrowth of the sidelobes, with the HFA3925 RFPA dominating the regrowth. This will result in maximum transmitted power available. To achieve this goal, once the PSK waveform is filtered at baseband, all remaining transmit elements are operated at a 6dB back-off from compression, except for the HFA3925 RFPA, which is operated at less back-off.

The low pass filters provide initial shaping of the PSK waveform. Final shaping is provided by a transmit IF filter, U5, a Toyocom TQS-432 SAW bandpass filter. The low pass filter outputs are off-chip AC coupled to the quadrature upconverter in the HFA3724. As in the receive mode, the baseband AC coupling time constant is approximately 25 times longer than the symbol period, and is implemented with $0.01 \mu \mathrm{~F}$ series capacitors. The same twice IF frequency LO used previously is also used in this up-conversion. The IF output of the HFA3724 is reactively matched to U5, with a $250 \Omega$ resistive load presented to the HFA3724. A shunt 33 nH inductor, in parallel with a $316 \Omega$ resistor, is used to provide this match, negate the effects of board and component capacitance, and provide a DC return to $\mathrm{V}_{\mathrm{CC}}$ to prevent saturation in the IF output stage of the HFA3724.

The output of U5 is terminated in a $200 \Omega$ potentiometer that is used for transmit gain control. A shunt 27 nH inductor is used to negate the effects of parasitic board and component shunt capacitance, as well as match the SAW output to the potentiometer. This potentiometer has it's center wiper connected to the HFA3624 RF/IF Converter transmit IF input, which has an input resistance of approximately $3 \mathrm{k} \Omega$. By varying the potentiometer, the gain of the transmit chain is controlled, allowing for precise control of the signal back-off at the HFA3925 RFPA. Therefore, this potentiometer is adjusted to achieve the desired compromise between transmit output power and the mainlobe to sidelobe ratio of the output PSK waveform, typically -32 dBc to -35 dBc , at an output power of +17.5 dBm .

Upconversion to the $2.4 \mathrm{GHz}-2.5 \mathrm{GHz}$ band is performed in the HFA3624 RF/IF Converter transmit mixer. The mixer output is filtered with FL2, a Murata LFJ30-03B2442B084 two pole monolithic LC bandpass filter. This filter suppresses the LO feedthrough from the mixer, and selects the upper sideband. The transmit buffer in the HFA3624 RF/IF Converter amplifies the selected sideband, easing the requirement for HFA3925 RFPA gain.

FL4, a Toko TDF2A-2450T-10 two pole dielectric bandpass filter, is used to further suppress both the transmit LO leakage and the undesired sideband.

The HFA3925 RFPA amplifies the transmit signal to a level of approximately +21.5 dBm , as measured at the $T / R$ switch output. This represents a back-off from 1 dB compression of approximately 3 dB . Transmit side-lobe performance is approximately -32 dBc to -35 dBc with this level of back-off. Allowing for approximately 4 dB of loss between the $\mathrm{T} / \mathrm{R}$
switch output and the antenna connector results in a final output power of +17.5 dBm .

The HFA3925 RFPA is the only physical layer component that operates directly from the 5V PC Card supply. To supply the needed negative gate bias to the HFA3925 RFPA, a ICL7660SIBA [8] charge pump is used. A second potentiometer is used to adjust the drain current on the third stage of the HFA3925 to a quiescent operating current of 90 mA , as measured through a one ohm sense resistor. A base-emitter junction is used as part of the gate bias network to provide temperature compensation, and all three gates are driven from one source to reduce the impact of process variation on pinch-off voltage. The nominal quiescent drain bias currents are 20 mA for stage one, 53 mA for stage two, and 90 mA for stage three.

A second logic-level PMOS switch, RF1K49093, is used to control the drain supply voltage to the HFA3925 RFPA, and implement a power down mode when receiving. A 2N2222 NPN transistor is used to level shift the 3.5 V logic level from the AM79C30 MAC to drive the 5V PMOS switch gates, as well as the 5V HFA3925 RFPA T/R control gate. The T/R $V_{D D}$ pin is connected to the three PA $V_{D D}$ pins, and is powered down in the receive mode by the PMOS switch. In this manner the T/R control pin transfer characteristic is less dependent on its voltage, with the receive state being valid for $T / R$ control voltages as low as $3 V$. If the $T / R V_{D D}$ pin was connected to a supply in both transmit and receive modes, the T/R control voltage would have to be within a few hundred millivolts of the supply to obtain similar performance.

Following the T/R switch, FL3 and FL6 are reused in the transmit mode to attenuate harmonics generated in the HFA3925 RFPA, as well as provide additional suppression of the LO. As the loss of FL3 and FL6 is approximately 4 dB , the amount of transmit power available at the antenna is approximately +17.5 dBm .

As the transmit chain is operated linearly, any gain flatness from the HFA3624 and HFA3925, as well as from FL2, FL3, FL4, and FL6, will result in the transmit output power varying across the operating channels. To reduce the amount of variability, three 1 pF capacitors are used as coupling elements to provide a form of simple equalization. Care must be exercised to ensure that the filter rejection is still acceptable in meeting the requirements of FCC 15.247. If desired, more complicated equalization could be used to maintain an improved $50 \Omega$ environment for all passband frequencies. Using the simple equalization, the transmit output varies approximately 2.5 dB across the band.

## Synthesizer Section

The dual frequency synthesizer section uses the HFA3524A [10] Synthesizer and two voltage controlled oscillators to provide a tunable 2132 MHz to 2204 MHz first LO, and a fixed 560 MHz second LO. Both feedback loops
use a 1 MHz reference frequency that is derived from a second 22 MHz Fox F4106 crystal oscillator. Two separate crystal oscillators were used for the HFA3824A and HFA3524A to maintain a high quality, low spurious reference for the synthesizer. Sharing a common 22 MHz oscillator is possible if care is taken to isolate the HFA3824A from the HFA3524A. Both feedback loops are third order and were designed to have loop bandwidths of 10 kHz , and phase margins of 50 degrees. The feedback loop analysis is included for both loops in Appendix D. Measured phase noise performance and calculated RMS phase jitter is included in Appendix E. All components in the synthesizer section operate from a regulated 3.5 V supply.

The tunable 2132 MHz to 2204 MHz first LO oscillator is a Motorola ${ }^{\text {TM }}$ KXN1332A VCO. To ensure operation at low tuning voltages, a start-up circuit was added to force the tuning voltage from the HFA3524A Synthesizer RF charge pump to a high state for a short period ( $\sim 1 \mathrm{~ms}$ ) following HFA3524A programming. A 2N2907 PNP transistor was used to implement this function, and the AM79C930 MAC device provides the control signal. The output level of the first LO to the HFA3624 RF/IF Converter is attenuated to approximately -3 dBm . An active buffer using an additional HFA3424 is used to provide additional isolation between the VCO and the HFA3624 LO input.

The fixed 560 MHz second LO oscillator is a discrete design, using a Phillips BFR505 transistor and a Siemens BBY51 varactor, as described in the HFA3524A Synthesizer evaluation board documentation. The output level of the second LO to the HFA3724 Quadrature IF
Modulator/Demodulator is attenuated to approximately -6dBm and a three pole low pass filter is included to preserve the duty cycle of the output. High even order components in the second LO can result in offsets from a $50 \%$ duty cycle, and will degrade the quadrature phase accuracy of the HFA3724. A transconductance network is used at the HFA3724 LO input to convert the second LO voltage into a current, as recommended in the HFA3724 data sheet. As the HFA3524A Synthesizer auxiliary IF input covers the 560 MHz range, the internal divide-by-two LO buffer output of the HFA3724 is disabled, as recommended in the HFA3724 data sheet.

## Regulator Section

Linear voltage regulators are used to provide filtering and isolation from the 5V PC Card input supply. An additional advantage of using voltage regulators is a savings in overall supply current, as all of the components that are regulated consume less current at a 3.5 V operating point, as opposed to a 5 V operating point. The 3.5 V operating point was chosen specifically to support the AM79C930 MAC controller. At the time of publication 3.5 V was the lowest nominal operating voltage approved by AMD for 40 MHz AM79C930 operation.

The only components operating directly from the 5 V supply are the HFA3925 RFPA, in order to maximize RF output power, and the PC Card interface sections of the AM79C930 MAC controller.

A total of three regulators, 3.5V Toko TK11235MTL, are used in the PC Card wireless LAN. One regulator supplies voltage to the HFA3824A Baseband Processor and portions of the AM79C930, as well as the HFA3424 LNA and HFA3624 RF/IF Converter. A second regulator supplies voltage to the synthesizer. The third regulator supplies voltage to the HFA3724 Quadrature IF Modulator/Demodulator.

## PCB Layout Guidelines

Although the actual PCB layout is proprietary, some of the techniques utilized are worthy of discussion [11]. As there are many RF, IF, analog, and digital circuits in close proximity, isolation is of prime concern. All RF and IF circuits utilize coplanar waveguide with ground transmission line techniques to allow for easy integration of varied line widths and component pin widths, and to provide a low dispersion, high isolation environment. A Radio Schematic is available on the internet at http://www.intersil.com.

The outside two planes of each side of the PCB are dedicated to RF and IF signal processing, and form two pairs of coplanar waveguide with ground circuits. As the two sides of the PCB contain circuitry that must be isolated from each other, blind via techniques are used, and the only places that the two sides share common ground or signal connections are when signals are passed between them - mainly when LO1 and LO2 need to pass from the synthesizer side to the RF/IF transceiver side.

In general, the RF and IF circuit layouts need to be as short and direct as possible to avoid costly shielding. This is especially critical in the receive IF stages where spurious signal coupling can easily occur, resulting in poor sensitivity or high packet error rates.

## Appendix A Reference Radio Bill Of Materials

table 2. REFERENCE RADIO BILL OF MATERIALS (Rev. A1, 3-26-98)

| LINE ITEM | PART \#/CUST. \# | VENDOR | VENDOR P/N | COMMODITY | TYPE | MECH. DES. MOIST. | REFERENCE DESCRIPTION | QTY | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | 00000003206C | Murata, AVX, Kemet, TDK | GRM39X7R104K016AD 0603YC104KAT2A C0603C104K5RAC C1608X7R1C104KT | Capacitor | Ceramic | SMT0603 | C21, C26, C27, C34, C36, C37, C38, C40, C41, C42, C45, C46, C53, C55, C57, C58, C66, C70, C71, C74, C79, C80, C82, C99, C101, C102, C106, C119, C120, C121, C124-C130, C132, C136 | 39 |  |
| 2 | 00000003209C | Motorola, Siemens | MMBT2907ALT1 SMBT2907A | Transistor | BJT-PNP | SMTSOT23 | Q4 | 1 |  |
| 3 | 00000004945C | Toko | LL1608-F15NK | Inductor | Power | SMT | L7, L9, L14, L23 | 4 |  |
| 4 | 00000006661C | Rohm | MCH212C683KP | Capacitor | Ceramic | SMT0805 | C97 | 1 |  |
| 5 | 00000009762C | Intersil | ICL7660SIBA-T | Linear | Converter | SMTSOIC N | U12 | 1 | Super Voltage Converter |
| 6 | 00000009897C | Siemens | BBY51-E6327 | Diode-Rect | Varactor | SMTSOT23 | CR3 | 1 | $\begin{aligned} & \mathrm{CT}=5.3 \mathrm{PF} \text { at } 1 \mathrm{~V}, \\ & \mathrm{CT}=3.1 \mathrm{PF} \text { at } 4 \mathrm{~V} \end{aligned}$ |
| 7 | 00000009898C | Dialight | 597-3401-407 | Optic | LED Single | SMT | DS2 | 1 | SMT, 7" Reel, 2500 Pieces/Reel |
| 8 | 00000009899C | Dialight | 597-3111-407 | Optic | LED Single | SMT | DS3 | 1 | SMT, 7" Reel, 2500 Pieces/Reel |
| 9 | 00000009900C | Intersil | HFA3724IN | Wireless/RF | Mod/Demod | TQFP Y -6 | U1 | 1 | 400 MHz Quadrature IF Modulator/Demod. |
| 10 | 00000009901C | Dialight | 597-3311-407 | Optic | LED Single | SMT | DS1 | 1 | SMT, 7" Reel, 2500 Pieces/Reel |
| 11 | 00000009902C | Intersil | HFA3624IA96 | Wireless/RF | Prescalar | SMTSSOP N | U4 | 1 | 2.4 GHz RF to IF Converter |
| 12 | 00000009903C | Philips | BFR 505 | Transistor | BJT-NPN | SMTSOT23 | Q2 | 1 | 9GHz Wideband Transistor, High Gain |
| 13 | 00000009904C | Toko | TK11235AMTL | Linear | Volt Reg | SMTSOT23 N | U13, U16, U21 | 3 | 3.5V Voltage Regulator with On/Off Switch |
| 14 | 00000009907C | AMD | AM79C930 | Controller |  | TQFP $\quad \mathrm{Y}$-4 | U3 | 1 | IC LAN Media Access Controller |
| 15 | 00000009935C | Toko | LL1608-F33NK | Inductor | Power | SMT0805 | L2, L4-L5 | 3 | Chip Inductor, $\mathrm{DCR}=0.65 \Omega$ |
| 16 | 00000009936C | AVX, TDK | 04025A5R6CAT2A C1005C0G1H5R6CT | Capacitor | Ceramic | SMT0402 | C78, C122 | 2 |  |
| 17 | 00000009937C | AVX, TDK | $\begin{aligned} & \text { 04025A4R7CAT2A } \\ & \text { C1005COG1H4R7CT } \end{aligned}$ | Capacitor | Ceramic | SMT0402 | C93 | 1 |  |
| 18 | 00000009938C | AVX, TDK | 04025C501JAT2A C1005X7R1H501JT | Capacitor | Ceramic | SMT0402 | C32, C154 | 2 |  |

TABLE 2. REFERENCE RADIO BILL OF MATERIALS (Rev. A1, 3-26-98) (Continued)

| LINE ITEM | PART \#/CUST. \# | VENDOR | VENDOR P/N | COMMODITY | TYPE | MECH. DES. MOIST. | REFERENCE DESCRIPTION | QTY | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 19 | 00000009943C | AVX, TDK | 04025A470JAT2A <br> C1005COG1H470JT | Capacitor | Ceramic | SMT0402 | C13, C18, C28, C60 | 4 |  |
| 20 | 00000009944C | AVX, TDK | 04025A100CAT2A <br> C1005COG1H100CT | Capacitor | Ceramic | SMT0402 | C31 | 1 |  |
| 21 | 00000009945C | AVX, TDK | 04025A101JAT2A C1005COG1H101JT | Capacitor | Ceramic | SMT0402 | C6, C9, C11, C12, C14, C15, C22, C30, C43, C47, C48, C65, C69, C72, C90, C92, C100, C104, C109, C110, C118 | 21 |  |
| 22 | 00000009947C | AVX, TDK | 0402YC103KAT*A C1005X7R1C103KT | Capacitor | Ceramic | SMT0402 | C1, C2, C3, C4, C5, C7, C8, C10, C16, C29, C35, C76, C94, C96, C147, C153 | 16 | * $=1,2, \mathrm{M}$ or N |
| 23 | 00000009948C | AVX, TDK | 04025A220JAT2A <br> C1005COG1H220JT | Capacitor | Ceramic | SMT0402 | $\begin{array}{\|l} \mathrm{C} 23, \mathrm{C} 24, \mathrm{C} 22, \mathrm{C} 67, \mathrm{C} 98, \\ \mathrm{C} 143 \end{array}$ | 6 |  |
| 24 | 00000009949C | AVX, TDK | 04023C102KAT2A <br> C1005X7R1C102KT | Capacitor | Ceramic | SMT0402 | C17, C19, C25, C33, C39, C50, C63, C64, C75, C95, C113, C138, C140, C141 | 14 |  |
| 25 | 00000009950C | Voltronics | JZ060 | Capacitor | Trim | SMT | C139 | 1 |  |
| 26 | 00000009974C | Panasonic, Rohm | ERJ2GEJ911X MCR01MZSJ911 | Resistor | Film | SMT0402 | R31 | 1 |  |
| 27 | 00000009975C | Panasonic, Rohm | $\begin{array}{\|l} \hline \text { ERJ2GEJ432X } \\ \text { MCR01MZ5J432 } \end{array}$ | Resistor | Film | SMT0402 | R63, R64 | 2 |  |
| 28 | 00000009976C | Panasonic, Rohm | ERJ2GEJ221X MCR01MZ5J221 | Resistor | Film | SMT0402 | R2, R33 | 2 |  |
| 29 | 00000009977C | Toko | TDF2A-2450T-10 | Filter | Dielectric | SMT | FL3-FL4, FL6 | 3 |  |
| 30 | 00000009978C | Panasonic, Rohm | ERJ2RKF2610X MCR01MZSF2610 | Resistor | Film | SMT0402 | R5 | 1 |  |
| 31 | 00000009979C | Panasonic, Rohm | ERJ2GEJ561X MCR01MZSJ561 | Resistor | Film | SMT0402 | R9 | 1 |  |
| 32 | 00000009981C | Panasonic, Rohm | ERJ2GEJ560X MCR01MZSJ560 | Resistor | Film | SMT0402 | R23, R87 | 2 |  |
| 33 | 00000009982C | Panasonic, Rohm | ERJ2GEJ472X MCR01MZSJ472 | Resistor | Film | SMT0402 | R38, R76 | 2 |  |
| 34 | 00000009983C | Panasonic | ERJ2GEJ153X | Resistor | Film | SMT0402 | R46, R77 | 2 |  |
| 35 | 00000009983C | Rohm | MCR01MZSJ153 | Resistor | Film | SMT0402 | R99-R104 | 6 |  |
| 36 | 00000009984C | Panasonic, Rohm | ERJ2GEJ104X MCR01M2SJ104 | Resistor | Film | SMT0402 | R27 | 1 |  |

table 2. REFERENCE RADIO BILL OF MATERIALS (Rev. A1, 3-26-98) (Continued)

| LINE ITEM | PART \#/CUST. \# | VENDOR | VENDOR P/N | COMMODITY | TYPE | MECH. DES. MOIST. | REFERENCE DESCRIPTION | QTY | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 37 | 00000009986C | Panasonic, Rohm | ERJ2GEJ152X MCR01MZSJ152 | Resistor | Film | SMT0402 | R35, R50 | 2 |  |
| 38 | 00000009989C | Panasonic, Rohm | ERJ2GEJ100X MCR01M2SJ100 | Resistor | Film | SMT0402 | R39, R85 | 2 |  |
| 39 | 00000009990C | Panasonic, Rohm | ERJ2GEJ101X MCR01M2SJ101 | Resistor | Film | SMT0402 | R45, R78 | 2 |  |
| 40 | 00000009991C | Panasonic, Rohm, K0A | ERJ2GEJ103X MCR01MZSJ103 RM73B1ET103J | Resistor | Film | SMT0402 | R41 | 1 |  |
| 41 | 00000009992C | Panasonic, Rohm | ERJ2GEJ750X MCR01MZSJ750 | Resistor | Film | SMT0402 | R51 | 1 |  |
| 42 | 00000009994C | Panasonic, Rohm | ERJ2GEJ681X MCR01MZSJ681 | Resistor | Film | SMT0402 | R42 | 1 |  |
| 43 | 00000010004C | Panasonic, Rohm | ERJ2GEJ392X MCR01MZSJ392 | Resistor | Film | SMT0402 | R13 | 1 | Resistor 3.9K 5\% 0402 1/16W |
| 44 | 00000010005C | Panasonic, Rohm | ERJ2GEJ822X MCR01MZSJ822 | Resistor | Film | SMT0402 | R22 | 1 | Resistor 8.2K 5\% 1/16W 0402 |
| 45 | 00000010006C | Panasonic, Rohm | ERJ2GEJ912X MCR01MZSJ912 | Resistor | Film | SMT0402 | R1 | 1 | Resistor 5\% 9.1K 1/16W 0402 |
| 46 | 00000010007C | Panasonic, Rohm | ERJ2GEJ331X MCR01MZSJ331 | Resistor | Film | SMT0402 | R21, R24 | 2 | Resistor 330 5 5\% 0402 |
| 47 | 00000010008C | Panasonic, Rohm | ERJ2GEJ102X MCR01MZSJ102 | Resistor | Film | SMT0402 | R4 | 1 | Resistor 1K 5\% 1/16W 0402 |
| 48 | 00000010009C | Panasonic, Rohm | ERJ2GE0R00X MCR01MZSJOR00 | Resistor | Film | SMT0402 | R7, R20, R48, R49, R55, R56, R59, R60, R61, R62, R66, R69, R97 | 13 | Resistor $0 \Omega$ Jumper 0402 |
| 49 | 00000010010C | Panasonic, Rohm | ERJ3GSYJ681V MCR03EZHMJ681 | Resistor | Film | SMT0603 | R58, R65 | 2 |  |
| 50 | 00000010011C | Panasonic, Rohm, KO, Q Dale | ERJ3EKF3160V MCR03EZHMF3160 <br> RK73H1JTF3160 CRCW06033160FRT1 | Resistor | Film | SMT0603 | R17 | 1 |  |
| 51 | 00000010012C | Rohm, Panasonic | MCR10EZHMJW331 ERJGEYJ331V | Resistor | Film | SMT0805 | R32 | 1 |  |
| 52 | 00000010013C | Philips | 9C06031A1R0F | Resistor | Film | SMT0603 | R3 | 1 | This was changed from the SMT0505 |
| 53 | 00000010014C | Intersil | HFA3524AIA96 | Wireless/RF | Synth | TSOP II N | U22 | 1 | $2.5 \mathrm{GHz} / 600 \mathrm{MHz}$ Dual Freq Synth. |
| 54 | 00000010021C | Intersil | HFA3824AVI | Wireless/RF | BBP | TQFP Y -2 | U6 | 1 | Baseband processor |

TABLE 2. REFERENCE RADIO BILL OF MATERIALS (Rev. A1, 3-26-98) (Continued)

| LINE ITEM | PART \#/CUST. \# | VENDOR | VENDOR P/N | COMMODITY | TYPE | MECH. DES. MOIST. | REFERENCE DESCRIPTION | QTY | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 55 | 00000010085C | NIC | NCB1206B320TR | Inductor | Ferr Chip | SMT | $\begin{aligned} & \text { L1, L8, L12, L19, L21, L22, } \\ & \text { L24 } \end{aligned}$ | 7 |  |
| 56 | 00000010169C | Intersil | HFA3424IB96 | Wireless/RF | LNA | SMTSOIC N | U19, U24 | 2 | RF component, 2.5 GHz Low Noise Amplifier |
| 57 | 00000010170C | Intersil | HFA3925IA96 | Wireless/RF | PA | SMTSSOP N | AR1 | 1 | 2.4-2.5GHz 25MW RF Power Amplifier |
| 58 | 00000010171C | Murata | LFJ30-03B2442B084 | Filter | EMI | SMT | FL1-FL2 | 2 | Tape and Reel 2.442GHz, $B W=84 \mathrm{MHz}$ |
| 59 | 00000010172C | Panasonic, Rohm | $\begin{aligned} & \hline \text { ERJ2RKF4990X } \\ & \text { MCR01MZSF4990 } \end{aligned}$ | Resistor | Film | SMT0402 | R10 | 1 | $\begin{aligned} & \text { Resistor, } 499 \Omega 1 \% 1 / 16 \mathrm{~W} \\ & 0402 \end{aligned}$ |
| 60 | 00000010214C | Statek | CX-6V-SM2-32.768K- | Freq Control | Crystal | SMT | U11 | 1 | Nickel tin plated termination |
| 61 | 00000011540C | Intersil | RF1K4909396 | Transistor | FET P-CH | SMTSO8 | U9, U25 | 2 | Dual MOSFET, 8 Pin DIL SMT package |
| 62 | 00000011729C | Panasonic, Rohm | $\begin{aligned} & \text { ERJ2GEJ751X } \\ & \text { MCR01MZSJ751 } \end{aligned}$ | Resistor | Film | SMT0402 | R26, R52 | 2 | $\begin{aligned} & \text { Resistor, } 750 \Omega 5 \% 0402 \\ & 1 / 16 \mathrm{~W} \end{aligned}$ |
| 63 | 00000011734C | Panasonic | EVM1SSW50B22 | Resistor | Pots | SMT | R19 | 1 |  |
| 64 | $\begin{aligned} & \text { 00000011758C } \\ & \text { None } \end{aligned}$ | AVX, TDK | 04025C222JAT2A C1005X7R1H222JT | Capacitor | Ceramic | SMT0402 | C142 | 1 |  |
| 65 | $\begin{aligned} & \text { 00000011759C } \\ & \text { None } \end{aligned}$ | AVX, NIC | 04023A101FAT2A <br> NMC0402NPO101F025T | Capacitor | Ceramic | SMT0402 | $\begin{aligned} & \text { C44, C49, C54, C61, C111, } \\ & \text { C155 } \end{aligned}$ | 6 |  |
| 66 | $\begin{aligned} & 00000011760 \mathrm{C} \\ & \text { None } \end{aligned}$ | AVX, TDK | 04023A200FAT*A C1005COG1E200CT | Capacitor | Ceramic | SMT0402 | C62 | 1 | * $=1,2, \mathrm{M}$ or N for AVX P/N |
| 67 | $\begin{aligned} & \text { 00000011762C } \\ & \text { None } \end{aligned}$ | AVX, TDK, NIC | 04023A150FAT2A C1005COG1E150FT NMC0402NPO150F25TR | Capacitor | Ceramic | SMT0402 | C73, C77 | 2 |  |
| 68 | 00000011836C N/A | AVX | L0603100GFWTR | Inductor | Power | SMT0603 | L3 | 1 | RF IND. L at $450 \Omega$, DCR $=0.13 \Omega$ |
| 69 | 00000011837C N/A | AVX | L0603120GFWTR | Inductor | Power | SMT0603 | L17 | 1 | RF IND. L at $450 \Omega$, DCR $=0.20 \Omega$ |
| 70 | 00000011866C | Panasonic, Rohm | $\begin{aligned} & \text { ERJ3GSYK106V } \\ & \text { MCR03EZHUK106 } \end{aligned}$ | Resistor | Film | SMT0603 | R57 | 1 |  |
| 71 | 00000011869C | Panasonic, Rohm | $\begin{aligned} & \hline \text { ERJ2GEJ430X } \\ & \text { MCR01MZSJ430 } \end{aligned}$ | Resistor | Film | SMT0402 | R36 | 1 |  |
| 72 | 00000011870C | Panasonic, Rohm | $\begin{aligned} & \text { ERJ2GEJ240X } \\ & \text { MCR01MZSJ240 } \end{aligned}$ | Resistor | Film | SMT0402 | R47, R53 | 2 | Resistor, 24ת 5\% 0402 |
| 73 | 00000012189C | Samsung, Mitsubishi | KM62256CLTG-5L M5M5256CVP-55LL | Memory | SRAM | TSOP I Y-3 | U8 | 1 |  |

TABLE 2. REFERENCE RADIO BILL OF MATERIALS (Rev. A1, 3-26-98) (Continued)

| LINE ITEM | PART \#/CUST. \# | VENDOR | VENDOR P/N | COMMODITY | TYPE | MECH. DES. MOIST. | REFERENCE DESCRIPTION | QTY | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 74 | 00000012987C | Fox, Statek | F4106-22.000M CXOM10N22M(25PPM) | Freq Control Oscillator |  | SMT | U20, U23 | 2 |  |
| 75 | 00000012990C | Panasonic, Rohm | ERJ2RKF9090X MCR01MZSF9090 | Resistor | Film | SMT0402 | R34 | 1 | $\begin{aligned} & \text { Resistor, } 909 \Omega 1 \% 0402 \\ & 1 / 16 \mathrm{~W} \end{aligned}$ |
| 76 | 00000012992C | Panasonic, Rohm | ERJ2RKF3011X MCR01MZSF3011 | Resistor | Film | SMT0402 | R14, R25 | 2 | Resistor, 3.01K 1\% 1/16W |
| 77 | 00000013250C | Panasonic, Rohm | ERJ2RKF7150X MCR01MZSF7150 | Resistor | Film | SMT0402 | R43, R84 | 2 | Resistor, $715 \Omega$ 1\% 1/16W 0402 |
| 78 | 00000013251C | Panasonic, Rohm | ERJ2GEJ511X MCR01MZSJ511 | Resistor | Film | SMT0402 | R82 | 1 |  |
| 79 | 00000013303C |  |  | Sheet Metal | Bottom Shield |  | Bottom Shield | 1 |  |
| 80 | 00000013319C None | AVX, TDK | 04025A5R0CAT*A C1005COG1H5R0CT | Capacitor | Ceramic | SMT0402 | C123, C144, C151 | 3 | * $=1$ or 2 |
| 81 | 00000013325 C <br> None | AVX, TDK | 0402YC562JAT*A C1005X7R1C562JT | Capacitor | Ceramic | SMT0402 | C91 | 1 | * $=1$ or 2 |
| 82 | 00000013326C <br> None | AVX | 0805YC563JAT*A | Capacitor | Ceramic | SMT0805 | C115 | 1 | * $=1$ or 2 |
| 83 | 00000013327C | AVX, Kemet | TAJS475K6R3R T491S475K006AS | Capacitor | Tantalum | SMTS | $\begin{aligned} & \text { C51, C56, C83, C85, C133, } \\ & \text { C134 } \end{aligned}$ | 6 | Low Profile - 3216L |
| 84 | 00000013329C | AVX | TAJT475K010R | Capacitor | Tantalum | SMTT | C84, C135 | 2 |  |
| 85 | 00000013330C | AVX | TAJT106K010R | Capacitor | Tantalum | SMTT | C81 | 1 | 3528L - Low Profile |
| 86 | 00000013345C | Panasonic, Rohm | $\begin{aligned} & \text { ERJ2GEJ394X } \\ & \text { MCR01MZSJ394 } \end{aligned}$ | Resistor | Film | SMT0402 | R79 | 1 |  |
| 87 | 00000013875C | AVX, Kemet, Murata | 06035C682KAT*A C0603C682K5RAC GRM39X7R682K050\%\# | Capacitor | Ceramic | SMT0603 | C89 | 1 | $\begin{aligned} & *=1 \text { or } 2 \text { or } \mathrm{M}: \%=\mathrm{A} \text { or } \mathrm{B}: \\ & \#=\mathrm{D} \text { or } \mathrm{L} \end{aligned}$ |
| 88 | 00000014977C | AVX, Murata | 04025A1R0CAT*A GRM36COG1R0C050\%\# | Capacitor | Ceramic | SMT0402 | C59, C131, C137 | 3 | $\begin{aligned} & *=1 \text { or } 2 \text { or } \mathrm{M}, \%=\mathrm{A} \text { or } \mathrm{B}, \\ & \#=\mathrm{D} \text { or } \mathrm{L} \end{aligned}$ |
| 89 | 00000015327C | Statek Fox | CXO-M-10N-40MHz (100PPM) F3355-40MHz | Freq Control Oscillator |  | SMT | U10 | 1 |  |
| 90 | 00000016302C | Panasonic, Rohm | ERJ2GEJ680X MCR01MZSJ680 | Resistor | Film | SMT0402 | R86 | 1 |  |
| 91 | 00000016708C | Murata, TDK AVX | GRM39COG2R0C050A\# C1608COG1H020CT 06035A2R0CAT*A | Capacitor | Ceramic | SMT0603 | C116 | 1 | * $=1,2, \mathrm{M}$ or N ; \# = D or L |
| 92 | 00000016709C | Murata TDK <br> AVX | GRM36COG8R0C050A\# C1005COG1H080CT 04025A8R0CAT*A | Capacitor | Ceramic | SMT0402 | C68 | 1 | * $=1,2, \mathrm{M}$ or N ; \# = D or L |

TABLE 2. REFERENCE RADIO BILL OF MATERIALS (Rev. A1, 3-26-98) (Continued)

| LINE ITEM | PART \#/CUST. \# | VENDOR | VENDOR P/N | COMMODITY | TYPE | MECH. DES. MOIST. | REFERENCE DESCRIPTION | QTY | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 93 | 00000016710C | Toko | LL2012-F27NK | Inductor | Fixed | SMT0805 | L6 | 1 | Chip Inductor, DCR $=0.55 \Omega$ |
| 94 | 00000016812C | Panasonic | EVM1SSX50B53 | Resistor | Poteniometer | SMT | R75 | 1 | 5K SMP Pot, Type X 2000 per Reel |
| 95 | 00000017117C | Toyocom | TQS-432E-7R | Filter | Saw | SMT | U5, U7 | 2 | Tape and Reel |
| 96 | 00000017587C |  |  | Label Outline Drawing | General |  |  |  |  |
| 97 | 00000018647C | ITT-Cannon |  | Coverset (top and bottom) |  |  |  |  |  |
| 98 | 00000018864C |  |  | Sheet Metal | Top Shield |  | Top shield | 1 |  |
| 99 | 00000019393C | CTS | KXN1332A | Freq Control | Oscillator | SMT | U18 | 1 | Voltage Controlled, $2132-2204 \mathrm{MHz}$ range |
| 100 | 00000019584C |  |  | PCB |  |  | PRISM1BRD | 1 | Raw PC Board |
| 101 | 00000019598C |  |  | Coppertape top cut out |  |  |  |  |  |
| 102 | 00000019599C |  |  | Coppertape bottom cut out |  |  |  |  |  |
| 103 | 00000025454C | Panasonic, <br> Rohm, KOA | ERJ2GEJ202X <br> MCR01MZSJ202 <br> RM73B1ET202J | Resistor | Film | SMT0402 | R37 | 1 |  |
| 104 | 00000027262C | KOA, Rohm | RM73B1ET132J MCR01MZSJ132 | Resistor | Film | SMT0402 | R44 | 1 |  |
| 105 | 00000027369C | AVX, Murata TDK | $\begin{aligned} & \text { 04023C122JAT*A } \\ & \text { GRM36X7R122J025A\# } \\ & \text { C1005X7R1E122JT } \end{aligned}$ | Capacitor | Ceramic | SMT0402 | C86 | 1 | * $=1,2, \mathrm{M}$ or $\mathrm{N} ; \#=\mathrm{D}$ or L |
| 106 | 00000032228C | AMD | Device Driver | Device Driver | Software |  | April '98 Software Win95 Driver | 1 |  |
| 107 | 00000032227C | AMD | Firmware Version 1.6 or later |  | Firmware |  | Firmware Version 1.6 April '98 or later | 0 |  |
| 108 | 000000932607C | ITT-Cannon |  | Connector 68-pin PC card side | Terminal |  | P1 | 1 |  |
| 109 | 0000013H9703fP | Toko | LL1608-F12NK | Inductor | Fixed | SMT0603 | L15-L16 | 2 | ( $\pm 10 \%$ ) |
| 110 | 000000941687 | Motorola | MMBT2222ALT1 | Transistor | BJT-NPN | SMTSOT23 | Q3, Q5 | 2 |  |
| 111 | 000000943218 | AMD | AM29F010-55EC | Memory | Flash | TSOP I Y-3 | U2 | 1 | 32 Pin Standard TSOP |

## Appendix B Receive Mixer Spurious Analysis

SystemPlus 1.0 S/N 11158 Copyright (c) 1992-1993 Webb Laboratories All Rights Reserved PRISM Reference Radio, 08/29/1996, 16:08:48

Receive Crossover Responses in Receive Band (2400MHz to 2500MHz)
LO Level $=+7 \mathrm{dBm}$

IF FREQ
LO FREQ
RCV FREQ
SPUR FREQ
No spurs recorded.
PRISM Reference Radio, 08/29/1996, 16:08:50
Spurious Responses in 0MHz to 5000MHz Band (-90dBC Minimum)
LO Level $=+7 \mathrm{dBm}$
Fixed Bandpass Preselector
Band Edges are 2400 MHz and 2500 MHz
4 Section Butterworth - Corner Attenuation $=1 \mathrm{~dB}$
Ultimate Preselector Rejection $=80 \mathrm{~dB}$

| IF FREQ | LO FREQ | RCV FREQ | SPUR FREQ | M | $\underline{N}$ | MXR | FLT | TOT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 280.0000 | 2120.0000 | 2400.0000 | 2400.0000 | +1 | -1 | 0 | 1 | 1 |
| 280.0000 | 2120.0000 | 2400.0000 | 1840.0000 | -1 | +1 | 0 | 80 | 80 |
| 280.0000 | 2120.0000 | 2400.0000 | 2488.0000 | -5 | +6 | 90 | 0 | 90 |
| 280.0000 | 2120.0000 | 2400.0000 | 2426.6667 | -6 | +7 | 90 | 0 | 90 |
| 280.0000 | 2120.0000 | 2400.0000 | 2462.8571 | +7 | -8 | 90 | 0 | 90 |
| 280.0000 | 2130.0000 | 2410.0000 | 2410.0000 | +1 | -1 | 0 | 0 | 0 |
| 280.0000 | 2130.0000 | 2410.0000 | 1850.0000 | -1 | +1 | 0 | 80 | 80 |
| 280.0000 | 2130.0000 | 2410.0000 | 2438.3333 | -6 | +7 | 90 | 0 | 90 |
| 280.0000 | 2130.0000 | 2410.0000 | 2474.2857 | +7 | -8 | 90 | 0 | 90 |
| 280.0000 | 2140.0000 | 2420.0000 | 2420.0000 | +1 | -1 | 0 | 0 | 0 |
| 280.0000 | 2140.0000 | 2420.0000 | 1860.0000 | -1 | +1 | 0 | 80 | 80 |
| 280.0000 | 2140.0000 | 2420.0000 | 2450.0000 | -6 | +7 | 90 | 0 | 90 |
| 280.0000 | 2140.0000 | 2420.0000 | 2485.7143 | +7 | -8 | 90 | 0 | 90 |
| 280.0000 | 2140.0000 | 2420.0000 | 2405.7143 | -7 | +8 | 90 | 0 | 90 |
| 280.0000 | 2150.0000 | 2430.0000 | 2430.0000 | +1 | -1 | 0 | 0 | 0 |
| 280.0000 | 2150.0000 | 2430.0000 | 1870.0000 | -1 | +1 | 0 | 80 | 80 |
| 280.0000 | 2150.0000 | 2430.0000 | 2461.6667 | -6 | +7 | 90 | 0 | 90 |
| 280.0000 | 2150.0000 | 2430.0000 | 2417.1429 | -7 | +8 | 90 | 0 | 90 |
| 280.0000 | 2160.0000 | 2440.0000 | 2440.0000 | +1 | -1 | 0 | 0 | 0 |
| 280.0000 | 2160.0000 | 2440.0000 | 1880.0000 | -1 | +1 | 0 | 80 | 80 |
| 280.0000 | 2160.0000 | 2440.0000 | 2473.3333 | -6 | +7 | 90 | 0 | 90 |
| 280.0000 | 2160.0000 | 2440.0000 | 2428.5714 | -7 | +8 | 90 | 0 | 90 |
| 280.0000 | 2170.0000 | 2450.0000 | 2450.0000 | +1 | -1 | 0 | 0 | 0 |
| 280.0000 | 2170.0000 | 2450.0000 | 1890.0000 | -1 | +1 | 0 | 80 | 80 |
| 280.0000 | 2170.0000 | 2450.0000 | 2485.0006 | -6 | +7 | 90 | 0 | 90 |
| 280.0000 | 2170.0000 | 2450.0000 | 2440.0000 | -7 | +8 | 90 | 0 | 90 |

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| IF FREQ | LO FREQ | RCV FREQ | SPUR FREQ | M | $\underline{N}$ | MXR | FLT | TOT |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 280.0000 | 2180.0000 | 2460.0000 | 2460.0000 | +1 | -1 | 0 | 0 | 0 |
| 280.0000 | 2180.0000 | 2460.0000 | 1900.0000 | -1 | +1 | 0 | 80 | 80 |
| 280.0000 | 2180.0000 | 2460.0000 | 2273.3333 | +3 | -3 | 50 | 39 | 89 |
| 280.0000 | 2180.0000 | 2460.0000 | 2451.4286 | -7 | +8 | 90 | 0 | 90 |
| 280.0000 | 2190.0000 | 2470.0000 | 2470.0000 | +1 | -1 | 0 | 0 | 0 |
| 280.0000 | 2190.0000 | 2470.0000 | 1910.0000 | -1 | +1 | 0 | 80 | 80 |
| 280.0000 | 2190.0000 | 2470.0000 | 2283.3333 | +3 | -3 | 50 | 37 | 87 |
| 280.0000 | 2190.0000 | 2470.0000 | 2462.8571 | -7 | +8 | 90 | 0 | 90 |
| 280.0000 | 2200.0000 | 2480.0000 | 2480.0000 | +1 | -1 | 0 | 0 | 0 |
| 280.0000 | 2200.0000 | 2480.0000 | 1920.0000 | -1 | +1 | 0 | 80 | 80 |
| 280.0000 | 2200.0000 | 2480.0000 | 2293.3333 | +3 | -3 | 50 | 35 | 85 |
| 280.0000 | 2200.0000 | 2480.0000 | 2474.2857 | -7 | +8 | 90 | 0 | 90 |
| 280.0000 | 2210.0000 | 2490.0000 | 2490.0000 | +1 | -1 | 0 | 0 | 0 |
| 280.0000 | 2210.0000 | 2490.0000 | 1930.0000 | -1 | +1 | 0 | 80 | 80 |
| 280.0000 | 2210.0000 | 2490.0000 | 2303.3333 | +3 | -3 | 50 | 32 | 82 |
| 280.0000 | 2210.0000 | 2490.0000 | 2485.7143 | -7 | +8 | 90 | 0 | 90 |
| 280.0000 | 2220.0000 | 2500.0000 | 2500.0000 | +1 | -1 | 0 | 1 | 1 |
| 280.0000 | 2220.0000 | 2500.0000 | 1940.0000 | -1 | +1 | 0 | 79 | 79 |
| 280.0000 | 2220.0000 | 2500.0000 | 2360.0000 | +2 | -2 | 74 | 15 | 89 |
| 280.0000 | 2220.0000 | 2500.0000 | 2313.3333 | +3 | -3 | 50 | 30 | 80 |

TABLE 3. RECEIVE SPUR TABLE - LO POWER = 7dBm

| 15 | 99 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 14 | 99 | 99 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 13 | 90 | 99 | 90 |  |  |  |  | $\mathrm{IF}=\mid\left(\mathrm{M}^{*}\right.$ SPUR $) \pm\left(\mathrm{N}^{*} \mathrm{LO}\right) \mid$ |  |  |  |  |  |  |  |  |
| 12 | 99 | 99 | 99 | 99 |  |  |  |  |  |  |  |  |  |  |  |  |
| 11 | 90 | 99 | 90 | 95 | 90 |  |  |  |  |  |  |  |  |  |  |  |
| 10 | 99 | 99 | 99 | 99 | 99 | 99 |  |  |  |  |  |  |  |  |  |  |
| 9 | 90 | 95 | 90 | 90 | 90 | 99 | 90 |  |  |  |  |  |  |  |  |  |
| 8 | 99 | 95 | 99 | 95 | 99 | 95 | 99 | 95 |  |  |  |  |  |  |  |  |
| (M) 7 | 90 | 90 | 90 | 90 | 90 | 87 | 90 | 90 | 90 |  |  |  |  |  |  |  |
| 6 | 90 | 90 | 90 | 90 | 90 | 90 | 90 | 90 | 90 | 90 |  |  |  |  |  |  |
| 5 | 90 | 80 | 90 | 71 | 90 | 68 | 90 | 65 | 88 | 65 | 85 |  |  |  |  |  |
| 4 | 86 | 90 | 86 | 88 | 88 | 85 | 86 | 85 | 90 | 85 | 85 | 85 |  |  |  |  |
| 3 | 67 | 64 | 69 | 50 | 77 | 47 | 74 | 44 | 74 | 47 | 75 | 44 | 70 |  |  |  |
| 2 | 73 | 73 | 74 | 70 | 71 | 64 | 69 | 64 | 69 | 62 | 74 | 62 | 72 | 60 |  |  |
| 1 | 24 | 0 | 35 | 13 | 40 | 24 | 45 | 28 | 49 | 33 | 53 | 42 | 60 | 47 | 63 |  |
| 0 | --- | 26 | 35 | 39 | 50 | 41 | 53 | 49 | 51 | 42 | 62 | 51 | 60 | 47 | 77 | 50 |
|  | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|  |  |  |  |  |  |  |  | (N) |  |  |  |  |  |  |  |  |

## Appendix C IF SAW Filter Measured Data

Toyocom TQS-432E-7R, VHF-Range Wideband Low Loss SAW Filter

| SPECIFICATIONS (TENTATIVE) |  |
| :--- | :--- |
| Reference Frequency (fo): | 280 MHz |
| Passband: | $\mathrm{f}_{\mathrm{O}} \pm 8.5 \mathrm{MHz}$ |
| Maximum Insertion Loss in Passband: | 10 dB Max |
| Attenuation: | $\mathrm{f}_{\mathrm{O}} \pm 38.8 \mathrm{MHz}$ at 50 dB |
| Terminating Impedance: | $270 \Omega / /-5 \mathrm{pF}$ |
| Operating Temperature Range: | $-10^{\circ} \mathrm{C}$ to $50^{\circ} \mathrm{C}$ |
| Package: | $\mathrm{SS}-752 \mathrm{~A}$ |



FIGURE 3.


FIGURE 4. FREQUENCY RESPONSE


FIGURE 6. GROUP DELAY


FIGURE 2.


FIGURE 5. FREQUENCY RESPONSE


FIGURE 7. INPUT IMPEDANCE CHARACTERISTIC

## Appendix D Synthesizer Loop Analysis

A linear control system model of the phase feedback for a PLL in the locked state is shown in Figure 8. The open loop gain is the product of the phase detector gain ( $\mathrm{K}_{\mathrm{PD}}$ ), the VCO gain (KVCO/s), and the loop filter gain $\mathrm{Z}(\mathrm{s})$ divided by the gain of the feedback counter modulus ( N ). The passive loop filter configuration used is displayed in Figure 9.


FIGURE 8. PLL LINEAR MODEL


FIGURE 9. PASSIVE LOOP FILTER
This analysis calculates the loop filter components for the PRISM HFA3524A Dual PLL.
A. Schaldenbrand and R.D. Schultz, 5/8/96

Where:
LO1, 2132 MHz to 2204 MHz ,
$\mathrm{f}_{\text {loop }}$ is the desired bandwidth of the PLL, in Hz ,
$f_{\text {ref }}$ is the reference frequency of the loop, in Hz ,
$\phi$ is the desired phase margin of the PLL, in degrees,
Kvco is the VCO Tuning Voltage Constant in $\mathrm{Hz} / \mathrm{V}$,
Kpd is the Phase Detector Pump Constant in A/rad,
N is the divider ratio,
1.424 is a constant to account for impact of R3/C3 pole.


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Plots of the magnitude and phase of $\mathrm{GH}(\mathrm{k})$ are shown in Figures 10 and 11.


FIGURE 10.


FIGURE 11.

This analysis calculates the loop filter components for the PRISM HFA3524A Dual PLL.
A. Schaldenbrand and R.D. Schultz, 5/8/96

Where:
LO2, 560MHz,
$\mathrm{f}_{\text {loop }}$ is the desired bandwidth of the PLL, in Hz, $f_{\text {ref }}$ is the reference frequency of the loop, in Hz , $\phi$ is the desired phase margin of the PLL, in degrees,

Kvco is the VCO Tuning Voltage Constant in Hz/V, Kpd is the Phase Detector Pump Constant in A/rad,

N is the divider ratio,
1.424 is a constant to account for impact of R3/C3 pole.
$\mathrm{f}_{\text {loop }}:=10 \cdot 10^{3} \quad \omega_{\mathrm{p}}:=2 \cdot \pi \bullet \mathrm{f}_{\text {loop }} \quad \omega_{\mathrm{p}}=6.283 \cdot 10^{4}$
$\mathrm{f}_{\text {ref }}:=1 \cdot 10^{6} \quad \omega_{\mathrm{r}}:=2 \bullet \pi \bullet \mathrm{f}_{\text {ref }} \quad \omega_{\mathrm{r}}=6.283 \cdot 10^{6}$
$\phi:=50^{\circ} \quad \phi_{r}:=\left(\pi \cdot \frac{\phi}{180^{\circ}}\right)$
Kvco : $=13 \cdot 10^{6} \mathrm{Kvco}:=2 \cdot \pi \cdot \mathrm{Kvco} \quad \mathrm{Kvco}=8.168 \cdot 10^{7}$
$\mathrm{Kpd}:=0.004 \mathrm{Kpd}:=\frac{\mathrm{Kpd}}{2 \cdot \pi} \quad \mathrm{Kpd}=6.366 \cdot 10^{-4}$
$N:=560$
$\mathrm{T} 3:=\frac{1}{10 \bullet \omega_{\mathrm{p}}} \quad \omega_{\mathrm{p}}:=1.424 \bullet \omega_{\mathrm{p}}$
$\mathrm{T} 1:=\frac{\sec \left(\phi_{\mathrm{r}}\right)-\tan \left(\phi_{\mathrm{r}}\right)}{\omega_{\mathrm{p}}} \quad \mathrm{T} 1=4.068 \cdot 10^{-6}$
$\omega_{c}:=\frac{\tan \left(\phi_{r}\right) \bullet(T 1+T 3)}{\left[(T 1+T 3)^{2}+T 1 \bullet T 3\right]} \cdot\left[\sqrt{1+\left[\frac{(T 1+T 3)^{2}+T 1 \bullet T 3}{\left(\tan \left(\phi_{r}\right) \bullet(T 1+T 3)\right)^{2}}\right]}-1\right]$
$\mathrm{T} 2:=\left[\frac{1}{\omega_{\mathrm{c}}{ }^{2} \cdot(\mathrm{~T} 1+\mathrm{T} 3)}\right] \quad \mathrm{f}_{\mathrm{c}}:=\frac{\omega_{\mathrm{c}}}{2 \bullet \pi}$
$\mathrm{C} 1:=\left(\frac{\mathrm{T} 1 \cdot \mathrm{Kpd} \cdot \mathrm{Kvco}}{\mathrm{N} \cdot \mathrm{T} 2 \cdot \omega_{\mathrm{c}}{ }^{2}}\right) \cdot \sqrt{\frac{1+\left(\omega_{\mathrm{c}} \cdot \mathrm{T} 2\right)^{2}}{\left[\left[1+\left(\omega_{\mathrm{c}} \cdot \mathrm{T} 1\right)^{2}\right] \cdot\left[1+\omega_{\mathrm{C}}(\mathrm{T} 3)^{2}\right]\right]}}$
$\mathrm{C} 2:=\mathrm{C} 1 \cdot\left[\left(\frac{\mathrm{~T} 2}{\mathrm{~T} 1}\right)-1\right]$
$\mathrm{R} 2:=\frac{\mathrm{T} 2}{\mathrm{C} 2}$

## Loop Filter Component Values

$\mathrm{T} 1=4.068 \cdot 10^{-6}$
$\mathrm{T} 2=4.472 \cdot 10^{-5}$
T3 $=1.592 \cdot 10^{-6}$
$\mathrm{f}_{\mathrm{C}}=1 \cdot 10^{4}$
$C 1=6.149 \cdot 10^{-9}$
C1 : = $5600 \cdot 10^{-12}$
$\mathrm{C} 2=6.146 \cdot 10^{-8}$
C2 : $=0.056 \cdot 10^{-6}$
R2: = 750

Rules of thumb for selecting the values of the reference frequency suppression filter are:

1. Choose $\mathrm{C} 3<\mathrm{C} 1 / 10$

$$
\begin{array}{ll}
\mathrm{C} 3:=\frac{\mathrm{C} 1}{10} & \mathrm{R} 3:=\frac{\mathrm{T} 3}{\mathrm{C} 3} \\
\mathrm{R} 3=2.842 \cdot 10^{3} & \mathrm{C} 3=5.6 \cdot 10^{-10}
\end{array}
$$

2. Choose R3 > 2 • R2

R3: $=2 \cdot R 2$
$R 3=1.5 \cdot 10^{3}$
$R 3=1500$
$\mathrm{C} 3:=\frac{\mathrm{T} 3}{\mathrm{R} 3}$
$C 3=1.061 \cdot 10^{-9}$
$C 3:=1000 \cdot 10^{-12}$
$k=10 . .70$
$k p(k):=10^{\left(\frac{k}{10}\right)}$


FIGURE 12.

$$
\begin{aligned}
& \omega(\mathrm{k}):=2 \mathrm{j} \bullet \pi \bullet \mathrm{kp}(\mathrm{k}) \\
& \mathrm{GH}(\mathrm{k}):=\mathrm{Kpd} \bullet \mathrm{Kvco} \bullet \frac{1+\omega(\mathrm{k}) \bullet \mathrm{T} 2}{(\mathrm{C} 1 \bullet \mathrm{~N} \bullet \omega(\mathrm{k}) \bullet \overline{\omega(\mathrm{K})}) \cdot(1+\omega(\mathrm{k}) \bullet \mathrm{T} 1)} \\
& \text { - } \frac{\mathrm{T} 1}{\mathrm{~T} 2} \cdot\left[\frac{1}{(1+\omega(\mathrm{k}) \bullet \mathrm{T} 3)}\right] \\
& \text { MAGdb_GH(k) : }=20 \cdot \log (\mathrm{GH}(\mathrm{k}) \cdot \overline{\mathrm{GH}(\mathrm{k})}) \\
& \text { PHI_GH(k) : }=\operatorname{atan}\left(\frac{\operatorname{Im}(\mathrm{GH}(\mathrm{k}))}{\operatorname{Re}(\mathrm{GH}(\mathrm{k}))}\right) \\
& \text { f_GH(k) : }=\left(\frac{180 \bullet \text { PHI_GH(k) }}{\pi}\right)-180 \\
& \text { MAG_GH(k) : }=(\mathrm{GH}(\mathrm{k}) \bullet \overline{\mathrm{GH}(\mathrm{k})}) \quad \text { Phim }(\mathrm{k}):=180+\mathrm{f} \_\mathrm{GH}(\mathrm{k})
\end{aligned}
$$

Plots of the magnitude and phase of $\mathrm{GH}(\mathrm{k})$ are shown in Figures 12 and 13.


FIGURE 13.

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## Appendix E Synthesizer Phase Noise/Jitter Analysis

TABLE 4. PRISM 1 LO PHASE NOISE ANALYSIS

## PRISM 1 LO PHASE NOISE ANALYSIS

## 3/22/96 RDS <br> 2.1GHz LO MEASURED PERFORMANCE

| FREQ OFFSET | $\mathrm{dBc} / \mathrm{Hz}$ | NOTES | PHASE JITTER (RADIANS SQUARED) | PHASE JITTER (RMS DEGREES) |
| :--- | :--- | :--- | :--- | :--- |
| 10 K | -76.6 |  | $2.382 \mathrm{E}-04$ | 0.884 |
| 20 K | -81.8 |  | $1.243 \mathrm{E}-04$ | 0.639 |
| 50 K | -92.4 |  | $8.781 \mathrm{E}-05$ | 0.537 |
| 200 K | -97.6 | $1.782 \mathrm{E}-05$ | 0.242 |  |
| 300 K | -103.7 |  | $5.511 \mathrm{E}-06$ | 0.135 |
| 400 K | -107.6 |  | $7.919 \mathrm{E}-06$ | 0.161 |
| 750 K | -111.2 |  |  |  |
| Total |  |  | $4.816 \mathrm{E}-04$ | 1.257 |

560MHz LO MEASURED PERFORMANCE

| 10K | -83.5 | $4.051 \mathrm{E}-05$ | 0.365 |
| :---: | :---: | :---: | :---: |
| 20K | -90.5 | $1.768 \mathrm{E}-05$ | 0.241 |
| 50K | -102.1 | 3.865E-06 | 0.113 |
| 100K | -106 | $1.608 \mathrm{E}-05$ | 0.230 |
| >200K | -111 |  |  |
| Total |  | 7.814E-05 | 0.506 |
| "Assume worst case, RMS measured 2.1 GHz and 560 MHz LO " |  |  |  |
|  |  | PHASE JITTER (RADIANS SQUARED) | PHASE JITTER (RMS DEGREES) |
| 2.1 GHz LO |  | 4.816E-04 | 1.257 |
| 560 MHz LO |  | 7.814E-05 | 0.506 |
| Total |  | 5.597E-04 | 1.355 |

## Appendix F Gain Distribution/IF Limiting Analysis

The IF stage, including the limiters, is of a differential design to improve noise rejection and stability for these high gain stages. The RF front end, on the other hand, is single ended to reduce complexity. A receive chain block diagram is shown in Figure 14.

The minimum limiter 1 and 2 voltage gains are 39 dB at 2.7 V and 400 MHz . The radio design uses the part at a less extreme operating point of 3.5 V and 280 MHz where the minimum performance is 42 dB . The limiter 1 and 2 output limiting voltage is $200 \mathrm{mV} V_{\text {P-p }}$ into a differential $500 \Omega$ load. Using 3 dB loss in the limiter Bandpass Filter (BPF), the limiter chain (LIM1, BPF, LIM2) cascaded voltage gain is 81 dB , with typical performance above 90 dB . With a $200 \mathrm{mV} \mathrm{V}_{\mathrm{P}-\mathrm{P}}$ output, the input limiting voltage is $17.8 \mu \mathrm{~V}_{\mathrm{P}-\mathrm{P}}$ or -98 dBm at $250 \Omega$ source impedance.

This is calculated as follows: since the source and load impedances are different ( $250 \Omega$ vs $500 \Omega$ ) the input signal is calculated in terms of voltage. Remember that the limiter is a voltage gain device and so gain is independent of source impedance. Substitute the result of Equation 1 into Equation 2 and calculate $\mathrm{V}_{\mathrm{IN}}(\mathrm{P}-\mathrm{P})$.
gain $=10^{\left(\frac{\text { GAIN (dB) }}{20}\right)}$
$\mathrm{V}_{\text {OUT }}=$ gain $\bullet \mathrm{V}_{\text {IN }}$
Calculate the input power with a $250 \Omega$ impedance by using Equation 3 to get $\mathrm{V}_{\mathrm{RMS}}$ and then substitute into Equation 4 with $R=250 \Omega$ to get power in Watts. Equation 3 assumes a sinewave crest factor for the $\sqrt{2}$ term. Power in Watts is converted to dBm with Equation 5 to get -98 dBm input power at $250 \Omega$ source impedance.
$V_{R M S}=\frac{V_{P-P}}{2 \cdot \sqrt{2}}$
$\operatorname{Pwr}($ Watts $)=\frac{V_{\text {RMS }}^{2}}{R}$

$$
\begin{equation*}
\operatorname{Pwr}(\mathrm{dBm})=10 \log \left(\operatorname{Pwr}(\text { Watts }) \cdot 10^{3}\right) \tag{EQ.5}
\end{equation*}
$$

The limiters have a noise bandwidth of over 500 MHz and so the cascaded limiters will fully limit on their own noise, if no BPF is used between the stages. The thermal noise voltage delivered from the $250 \Omega$ source to the limiters in a 500 MHz band is -87 dBm , as calculated from Equation 6. This thermal noise adds to the limiter noise figure (NF) of 7dB resulting in an equivalent input noise power of -80 dBm , which is significantly higher than the -98 dBm required for limiting.
$P(\text { Watts })_{A}=k T \Delta f$

Where:

$$
\begin{aligned}
\mathrm{P}(\text { Watts })_{\mathrm{A}}= & \text { Available Noise Power } \\
\mathrm{k}= & 1.38042 \times 10^{-23} \\
& \text { Boltzmann's Constant } \\
\mathrm{T}= & 300 \text { Degree Kelvin } \\
\Delta \mathrm{f}= & 500 \mathrm{MHz}
\end{aligned}
$$

The RF front end 3dB bandwidth is 17 MHz , with an estimated noise bandwidth of 20 MHz , as defined by the IF SAW filter. This makes the available thermal noise at the limiter input -101 dBm and with the 7 dB limiter noise figure, is an equivalent -94 dBm .

If the limiter BPF was also 20 MHz , the front end would only need to supply 7 dB of noise floor gain to overcome the limiter noise figure. This would result in a receiver that limits in a 20 MHz bandwidth from front end noise with no margin. The 20 MHz limiter BPF would require a second SAW filter and therefore is not cost effective or practical.

The alternative chosen to be implemented is a simple one pole LC BPF with a bandwidth wide enough so that the variability of fixed components do not result in the filter being off frequency. The filter selected has a 3dB bandwidth of 50 MHz , and an estimated noise bandwidth of 100 MHz . Using this method, the front end gain must be increased to compensate for excess limiter bandwidth.


WHERE $^{\text {BW }}$ N $=$ NOISE BANDWIDTH

FIGURE 14. RECEIVE CHAIN GAIN DISTRIBUTION DIAGRAM

It is desired that the second limiter to be fully limited on front end noise, as opposed to noise generated in the first limiter. This requires that the front end noise floor must be greater than the sum of the following; the limiter NF of 7 dB , the ratio of limiter BPF noise bandwidth to front end IF SAW bandwidth $(10 \log (100 \mathrm{MHz} / 20 \mathrm{MHz})$ or 7 dB$)$, and the amount of limiting margin ( 6 dB for -1 dB limiting). The front end output noise floor must therefore be greater than 20 dB .
The limiting margin was measured on the HFA3724 IF Mod/Demod, with good agreement to a theoretical estimate based upon the hyperbolic tangent response of a bipolar differential limiter. The measurement means that if a nondesired jamming signal, noise in this case, is 6 dB below the level of the desired signal, the desired output will be reduced 1 dB .

The front end noise floor was previously calculated for a 20 MHz bandwidth as -101 dBm , if the required gain is now added, this noise floor becomes -81dBm as shown in Equation 7. Now verify that this level is larger than the minimum signal power required to limit the limiter chain and guarantee that the radio limits on front end noise ( $-81 \mathrm{dBm}>-98 \mathrm{dBm}$ ).
$(20 \mathrm{MHz} \mathrm{kTB})+\mathrm{NF}_{\text {LIM }}+$ BPF $_{\text {Noise }}$

+ Lim $_{\text {Margin }}=$ Front End Noise
i.e.
$-101 \mathrm{dBm}+7 \mathrm{~dB}+7 \mathrm{~dB}+6 \mathrm{~dB}=-81 \mathrm{dBm}$
Where;
( 20 MHz kTB ) is Available Thermal Noise
NF LIM is Noise Figure of Limiter Chain
BPF $_{\text {Noise }}$ is Added Noise due to Limiter BPF Bandwidth wider than Front End

Lim $_{\text {Margin }}$ is Front End Margin required to guarantee limiter jammer rejection

The actual front end gain is 13.4 dB and NF is 7.7 dB for a front end output noise floor increase of 21.1 dB typical, which is better than desired 20 dB . This results in limiting, when no signal is present, on mainly front end noise, but also some limiter broadband noise. This limiter output, although still fully limited, when band filtered will have a slight drop in baseband quadrature output voltage to the HFA3824A ADCs as compared to totally limiting on front end noise due to some of the limiter noise being out of band. The net impact to the system is a small reduction in sensitivity due to reduced ADC signal to full scale. If desired, additional front end gain, or a reduced bandwidth limiter BPF could be used to gain back performance.

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