TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC4027BP, TC4027BF

TC4027B Dual J-K Master-Slave Flip Flop

TC4027B is J-K master-slave flip-flop having RESET and SET functions.

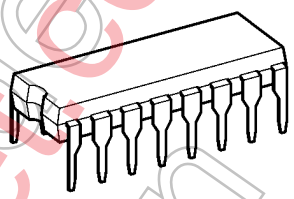
In the case of J-K made, when the clock input is given with both RESET and SET at "L", the output changes at rising edge of the clock according to the states of J and K.

When SET input is placed at "H", and RESET input is placed at "L", outputs become Q = "H", and $\overline{Q}$ = "L".

When RESET input is placed at "H", and SET input is placed at "L", outputs become Q = "L", and $\overline{Q}$ = "H".

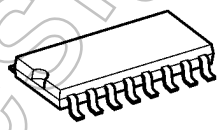
When both of RESET input and SET input are at "H", outputs become Q = "H" and $\overline{Q}$ = "H".

TC4027BP



DIP16-P-300-2.54A

TC4027BF



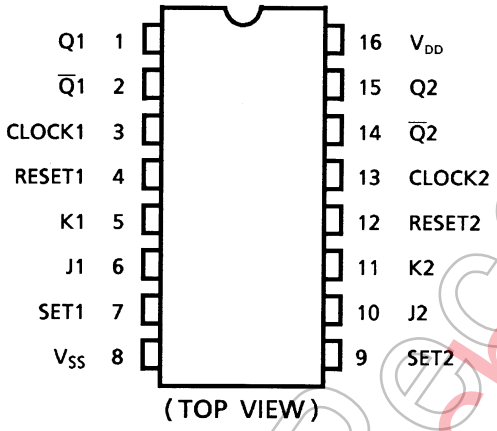
SOP16-P-300-1.27A

Weight

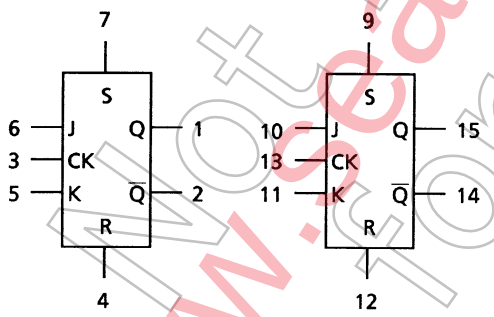
DIP16-P-300-2.54A : 1.00 g (typ.)

SOP16-P-300-1.27A : 0.18 g (typ.)

Pin Assignment



Block Diagram



Start of commercial production
1985-02

Truth Table

Inputs					Outputs	
RESET	SET	J	K	CLOCK∆	Q_{n+1}	$\overline{Q}_{n+1}$
L	H	*	*	*	H	L
H	L	*	*	*	L	H
H	H	*	*	*	H	H
L	L	L	L	↑	Q_n*	Q_n*
L	L	L	H	↑	L	H
L	L	H	L	↑	H	L
L	L	H	H	↑	$\overline{Q}_n$ **	Q_n**
L	L	*	*	↓	Q_n*	$\overline{Q}_n$ *

*: Don't care

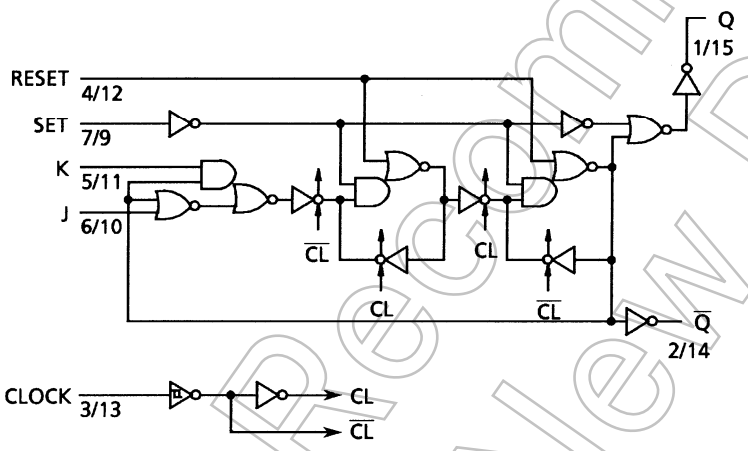
∆: Level change

*: No change

**: Change

Logic Diagram

1/2 TC4027B



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
DC supply voltage	V_{DD}	V_{SS} − 0.5 to V_{SS} + 20	V
Input voltage	V_{IN}	V_{SS} − 0.5 to V_{DD} + 0.5	V
Output voltage	V_{OUT}	V_{SS} − 0.5 to V_{DD} + 0.5	V
DC input current	I_{IN}	±10	mA
Power dissipation	P_D	300 (DIP)/180 (SOP)	mW
Operating temperature range	T_{opr}	−40 to 85	°C
Storage temperature range	T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (V_{SS} = 0 V) (Note)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
DC supply voltage	V_{DD}	—	3	—	18	V
Input voltage	V_{IN}	—	0	—	V_{DD}	V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{DD} or V_{SS}.

Static Electrical Characteristics (V_{SS} = 0 V)

Characteristics	Sym-bol	Test Condition		−40°C		25°C			85°C		Unit
			V_{DD} (V)	Min	Max	Min	Typ.	Max	Min	Max	
High-level output voltage	V_{OH}	$\|I_{OUT}\| < 1$ μA $V_{IN} = V_{SS}, V_{DD}$	5	4.95	—	4.95	5.00	—	4.95	—	V
			10	9.95	—	9.95	10.00	—	9.95	—	
			15	14.95	—	14.95	15.00	—	14.95	—	
Low-level output voltage	V_{OL}	$\|I_{OUT}\| < 1$ μA $V_{IN} = V_{SS}, V_{DD}$	5	—	0.05	—	0.00	0.05	—	0.05	V
			10	—	0.05	—	0.00	0.05	—	0.05	
			15	—	0.05	—	0.00	0.05	—	0.05	
Output high current	I_{OH}	V_{OH} = 4.6 V	5	−0.61	—	−0.51	−1.0	—	−0.42	—	mA
		V_{OH} = 2.5 V	5	−2.50	—	−2.10	−4.0	—	−1.70	—	
		V_{OH} = 9.5 V	10	−1.50	—	−1.30	−2.2	—	−1.10	—	
		V_{OH} = 13.5 V	15	−4.00	—	−3.40	−9.0	—	−2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Output low current	I_{OL}	V_{OL} = 0.4 V	5	0.61	—	0.51	1.2	—	0.42	—	mA
		V_{OL} = 0.5 V	10	1.50	—	1.30	3.2	—	1.10	—	
		V_{OL} = 1.5 V	15	4.00	—	3.40	12.0	—	2.80	—	
		$V_{IN} = V_{SS}, V_{DD}$									
Input high voltage	V_{IH}	V_{OUT} = 0.5 V, 4.5 V	5	3.5	—	3.5	2.75	—	3.5	—	V
		V_{OUT} = 1.0 V, 9.0 V	10	7.0	—	7.0	5.50	—	7.0	—	
		V_{OUT} = 1.5 V, 13.5 V	15	11.0	—	11.0	8.25	—	11.0	—	
		$\|I_{OUT}\| < 1$ μA									
Input low voltage	V_{IL}	V_{OUT} = 0.5 V, 4.5 V	5	—	1.5	—	2.25	1.5	—	1.5	V
		V_{OUT} = 1.0 V, 9.0 V	10	—	3.0	—	4.50	3.0	—	3.0	
		V_{OUT} = 1.5 V, 13.5 V	15	—	4.0	—	6.75	4.0	—	4.0	
		$\|I_{OUT}\| < 1$ μA									
Input current "H" level	I_{IH}	V_{IH} = 18 V	18	—	0.1	—	10^{-5}	0.1	—	1.0	μA
Input current "L" level	I_{IL}	V_{IL} = 0 V	18	—	−0.1	—	-10^{-5}	−0.1	—	−1.0	
Quiescent supply current	I_{DD}	$V_{IN} = V_{SS}, V_{DD}$ (Note)	5	—	1	—	0.002	1	—	30	μA
			10	—	2	—	0.004	2	—	60	
			15	—	4	—	0.008	4	—	120	

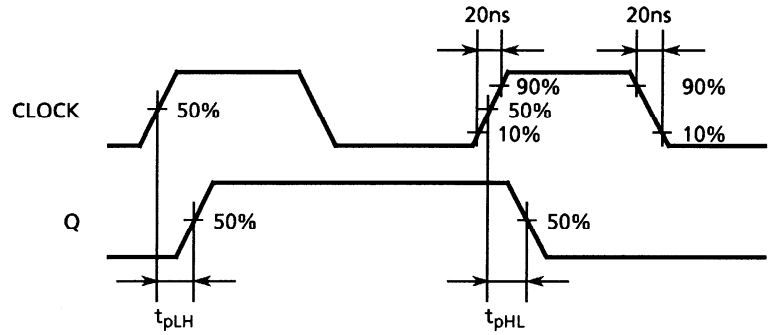
Note: All valid input combinations.

Dynamic Electrical Characteristics (Ta = 25°C, V_{SS} = 0 V, C_L = 50 pF)

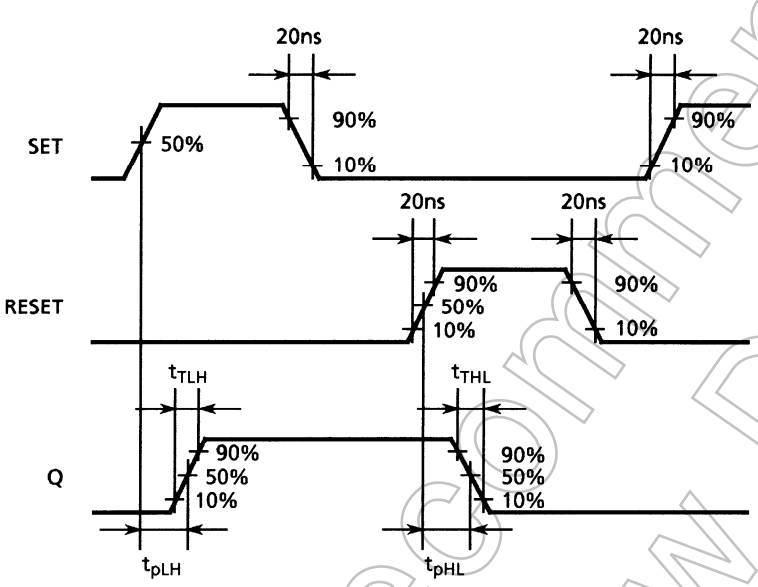
Characteristics	Symbol	Test Condition	V_{DD} (V)	Min	Typ.	Max	Unit
Output transition time (low to high)	t_{TLH}	—	5	—	70	200	ns
			10	—	35	100	
			15		30	80	
Output transition time (high to low)	t_{THL}	—	5	—	70	200	ns
			10	—	35	100	
			15	—	30	80	
Propagation delay time (CLOCK-Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	5	—	150	300	ns
			10	—	75	130	
			15	—	60	90	
Propagation delay time (SET, RESET-Q, $\overline{Q}$)	t_{pLH} t_{pHL}	—	5	—	120	300	ns
			10	—	60	130	
			15	—	45	90	
Max clock frequency	f_{CL}	—	5	3.5	8	—	MHz
			10	8.0	16	—	
			15	12.0	20	—	
Max clock input rise time Max clock input fall time	t_{rCL} t_{fCL}	—	5 10 15	No limit			μs
Min pulse width (SET, RESET)	t_W	—	5	—	60	180	ns
			10	—	35	80	
			15	—	25	50	
Min clock pulse width	t_W	—	5	—	60	140	ns
			10	—	35	60	
			15	—	25	40	
Min set-up time (J, K-CLOCK)	t_{SU}	—	5	—	30	140	ns
			10	—	10	50	
			15	—	5	35	
Min hold time (J, K-CLOCK)	t_H	—	5	—	—	140	ns
			10	—	—	50	
			15	—	—	35	
Min removal time (SET, RESET-CLOCK)	t_{rem}	—	5	—	—	40	ns
			10	—	—	20	
			15	—	—	15	
Input capacitance	C_{IN}	—		—	5	7.5	pF

Waveforms for Measurement of Dynamic Characteristics

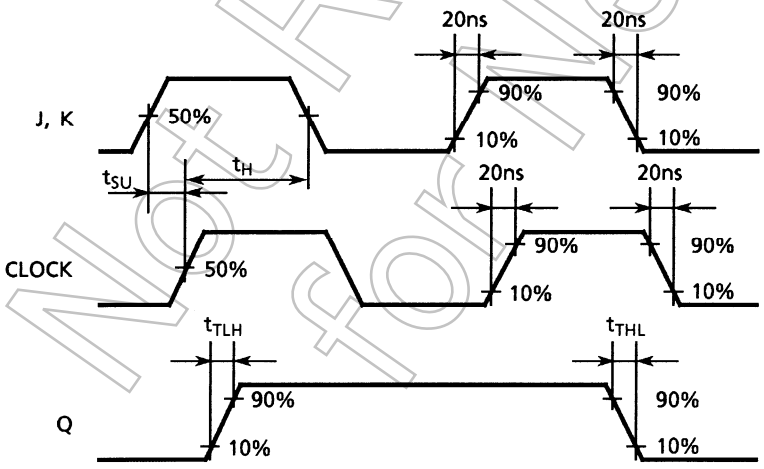
Waveform 1



Waveform 2

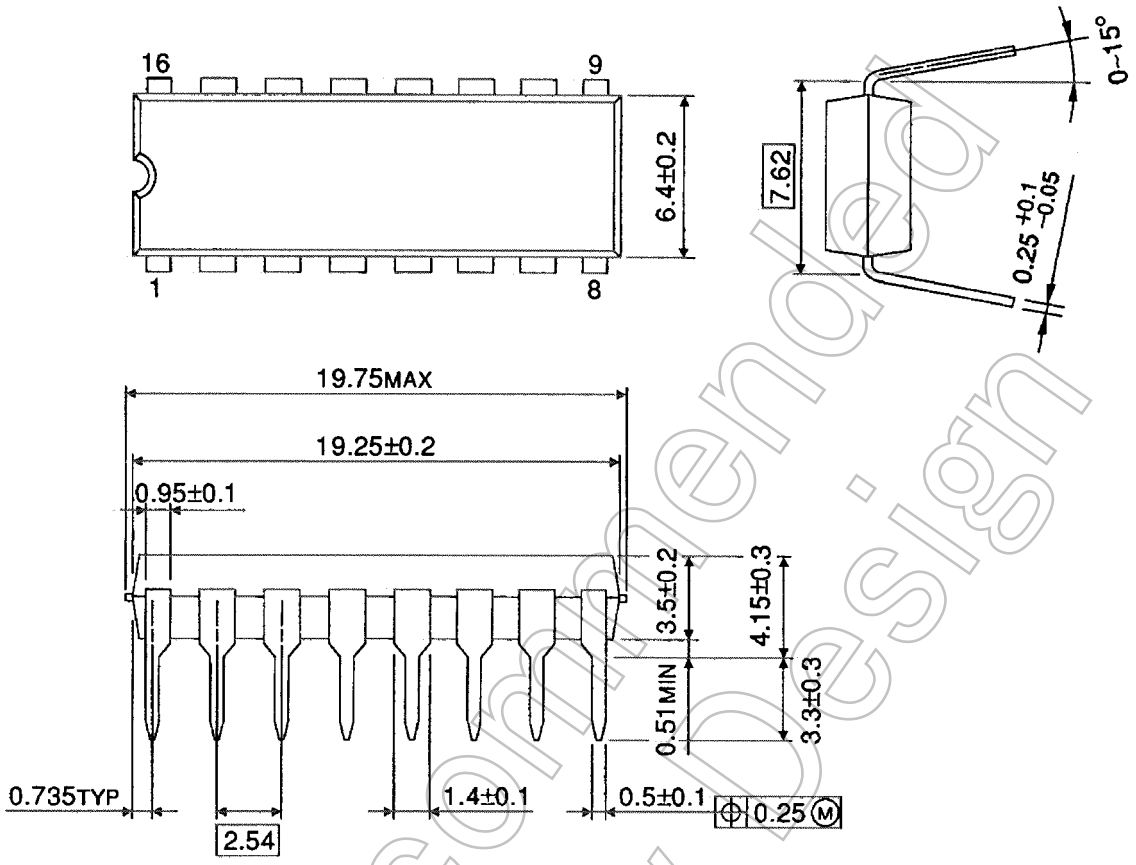


Waveform 3



Package Dimensions

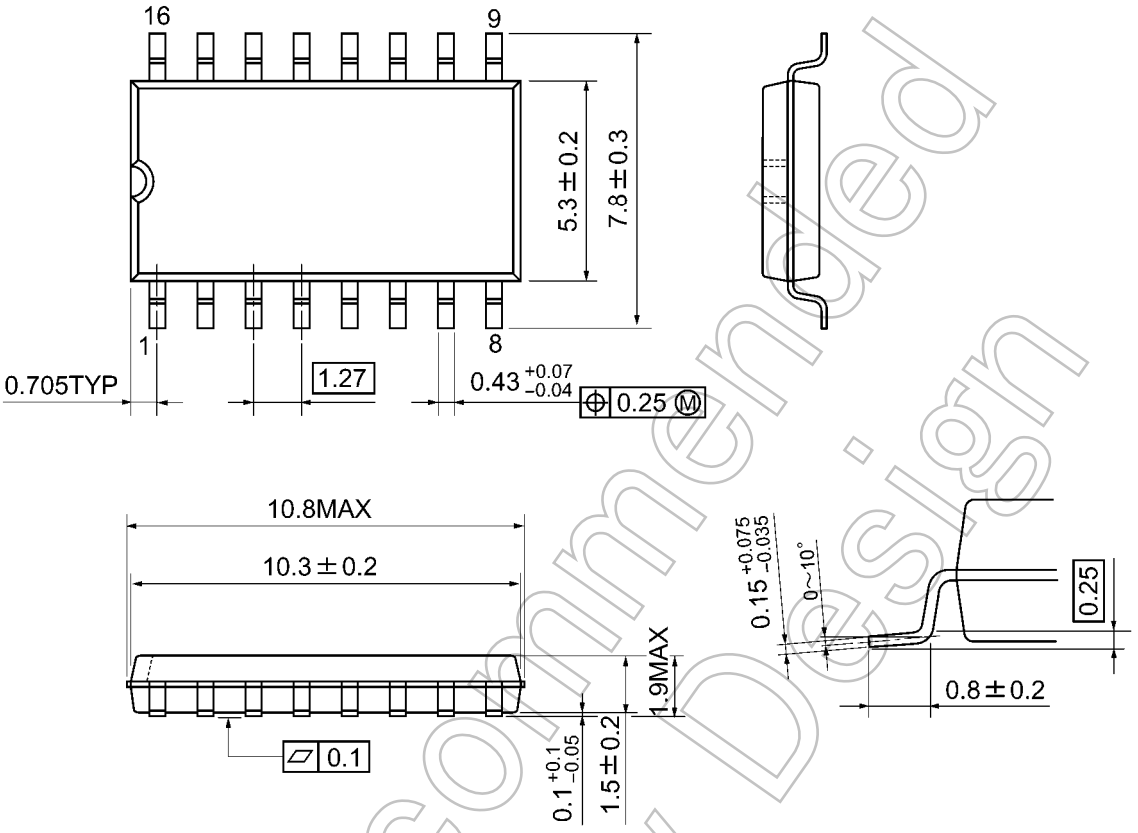
DIP16-P-300-2.54A Unit : mm



Weight: 1.00 g (typ.)

Package Dimensions

SOP16-P-300-1.27A Unit: mm



Weight: 0.18 g (typ.)

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