

## 74LCX16543

# Low-Voltage 16-Bit Registered Transceiver with 5V-Tolerant Inputs and Outputs

### General Description

The LCX16543 contains sixteen non-inverting transceivers containing two sets of D-type registers for temporary storage of data flowing in either direction. Each byte has separate control inputs which can be shorted together for full 16-bit operation. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow.

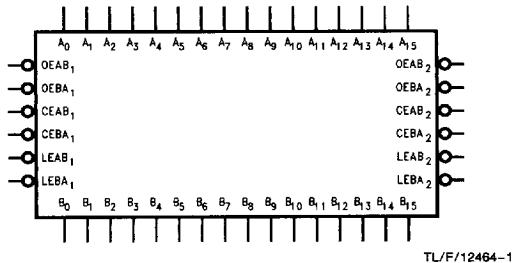
The LCX16543 is designed for low voltage (3.3V) V<sub>CC</sub> applications with capability of interfacing to a 5V signal environment.

The LCX16543 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

### Features

- 5.2 ns t<sub>PD</sub> max, 20  $\mu$ A I<sub>CCQ</sub> max
- 5V tolerant inputs and outputs
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal
- 2.0V–3.6V V<sub>CC</sub> supply operation
- $\pm 24$  mA output drive
- Implements patented Quiet Series™ noise/EMI reduction circuitry
- Functionally compatible with the 74 series 16543
- Latch-up performance exceeds 500 mA
- ESD performance:  
Human Body Model > 2000V  
Machine Model > 200V

### Logic Symbol

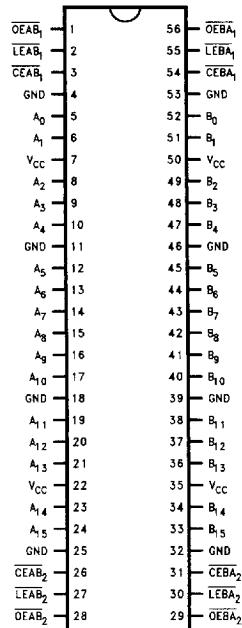


Pin Names	Description
OEAB <sub>n</sub>	A-to-B Output Enable Input (Active LOW)
OEBA <sub>n</sub>	B-to-A Output Enable Input (Active LOW)
CEAB <sub>n</sub>	A-to-B Enable Input (Active LOW)
CEBA <sub>n</sub>	B-to-A Enable Input (Active LOW)
LEAB <sub>n</sub>	A-to-B Latch Enable Input (Active LOW)
LEBA <sub>n</sub>	B-to-A Latch Enable Input (Active LOW)
A <sub>0</sub> -A <sub>15</sub>	A-to-B Data Inputs or B-to-A TRI-STATE® Outputs
B <sub>0</sub> -B <sub>15</sub>	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

	SSOP	TSSOP
Order Number	74LCX16543MEA 74LCX16543MEAX	74LCX16543MTD 74LCX16543MTDX
See NS Package Number	MS56A	MTD56

### Connection Diagram

Pin Assignment for SSOP and TSSOP



## Functional Description

The 'LCX16543 contains sixteen non-inverting transceivers with TRI-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The following description applies to each byte. For data flow from A to B, for example, the A-to-B Enable ( $\overline{CEAB}_n$ ) input must be LOW in order to enter data from  $A_0-A_{15}$  or take data from  $B_0-B_{15}$ , as indicated in the Data I/O Control Table. With  $\overline{CEAB}_n$  LOW, a LOW signal on the A-to-B Latch Enable ( $LEAB_n$ ) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the  $LEAB_n$  signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With  $\overline{CEAB}_n$  and  $\overline{OEAB}_n$  both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the  $CEBA_n$ ,  $LEBA_n$  and  $OEBA_n$  inputs.

Data I/O Control Table

Inputs			Latch Status (Byte n)	Output Buffers (Byte n)
$CEAB_n$	$LEAB_n$	$OEAB_n$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

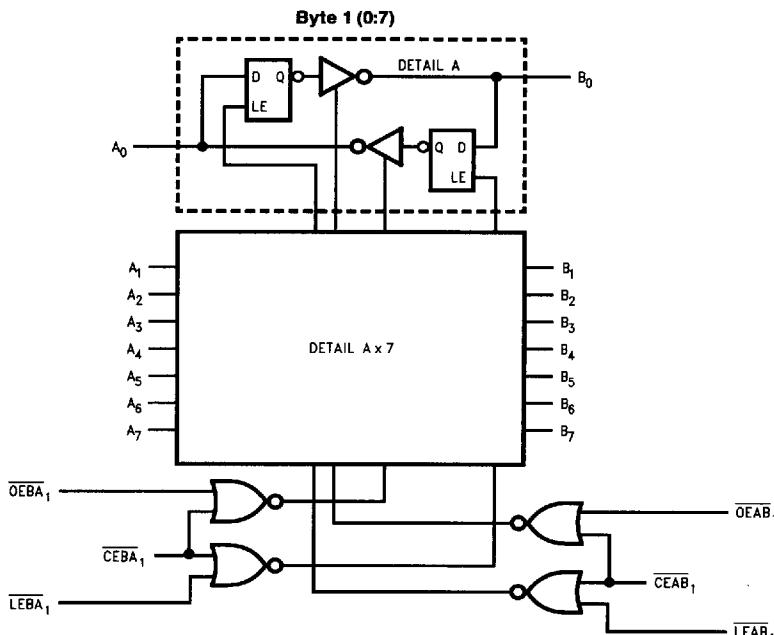
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

A-to-B data flow shown; B-to-A flow control is the same, except using  $CEBA_n$ ,  $LEBA_n$  and  $OEBA_n$ 

## Logic Diagrams

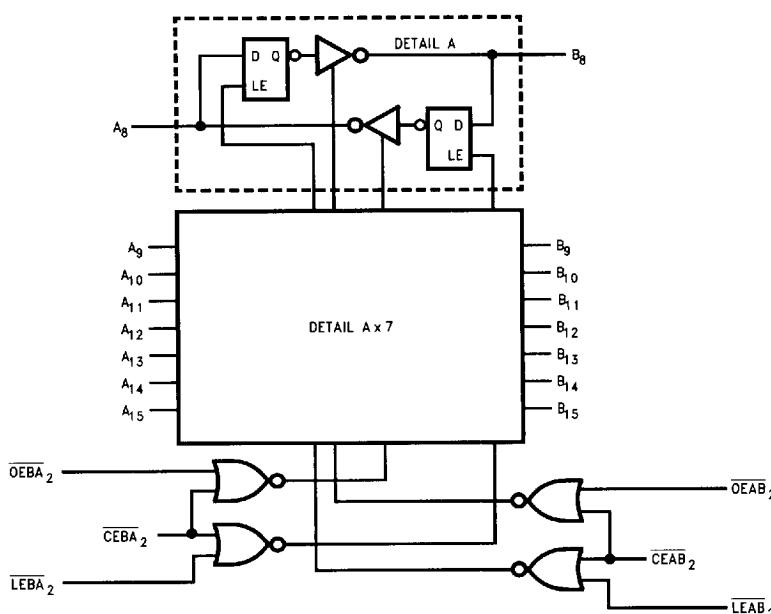


TL/F/12464-3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Logic Diagrams (Continued)

Byte 2 (8:15)



TL/F/12464-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Symbol	Parameter	Value	Conditions	Units
$V_{CC}$	Supply Voltage	-0.5 to +7.0		V
$V_I$	DC Input Voltage	-0.5 to +7.0		V
$V_O$	DC Output Voltage	-0.5 to +7.0	Output in TRI-STATE	V
		-0.5 to $V_{CC} + 0.5$	Output in High or Low State (Note 2)	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50 +50	$V_O < GND$ $V_O > V_{CC}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature	-65 to +150		°C

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2:  $I_O$  Absolute Maximum Rating must be observed.

## Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V <sub>CC</sub>	Supply Voltage	Operating Data Retention	2.0 1.5	3.6 3.6	V
V <sub>I</sub>	Input Voltage		0	5.5	V
V <sub>O</sub>	Output Voltage	HIGH or LOW State TRI-STATE	0 0	V <sub>CC</sub> 5.5	V
I <sub>OH</sub> /I <sub>OL</sub>	Output Current	V <sub>CC</sub> = 3.0V – 3.6V V <sub>CC</sub> = 2.7V		±24 ±12	mA
T <sub>A</sub>	Free-Air Operating Temperature		-40	85	°C
Δt/ΔV	Input Edge Rate, V <sub> N</sub> = 0.8V–2.0V, V <sub>CC</sub> = 3.0V		0	10	ns/V

## DC Electrical Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C		Units
				Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage		2.7–3.6	2.0		V
V <sub>IL</sub>	LOW Level Input Voltage		2.7–3.6		0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	I <sub>OH</sub> = -100 μA	2.7–3.6	V <sub>CC</sub> – 0.2		V
		I <sub>OH</sub> = -12 mA	2.7	2.2		V
		I <sub>OH</sub> = -18 mA	3.0	2.4		V
		I <sub>OH</sub> = -24 mA	3.0	2.2		V
V <sub>OL</sub>	LOW Level Output Voltage	I <sub>OL</sub> = 100 μA	2.7–3.6		0.2	V
		I <sub>OL</sub> = 12 mA	2.7		0.4	V
		I <sub>OL</sub> = 16 mA	3.0		0.4	V
		I <sub>OL</sub> = 24 mA	3.0		0.55	V
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>I</sub> ≤ 5.5V	2.7–3.6		±5.0	μA
I <sub>OZ</sub>	TRI-STATE I/O Leakage	0 ≤ V <sub>O</sub> ≤ 5.5V V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	2.7–3.6		±5.0	μA
I <sub>OFF</sub>	Power-Off Leakage Current	V <sub>I</sub> or V <sub>O</sub> = 5.5V	0		10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>I</sub> = V <sub>CC</sub> or GND	2.7–3.6		20	μA
		3.6V ≤ V <sub>I</sub> , V <sub>O</sub> ≤ 5.5V	2.7–3.6		±20	μA
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	V <sub>IH</sub> = V <sub>CC</sub> – 0.6V	2.7–3.6		500	μA

## AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$				Units	
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$			
		Min	Max	Min	Max		
$t_{PHL}$	Propagation Delay $A_n$ to $B_n$ or $B_n$ to $A_n$	1.5 1.5	5.2 5.2	1.5 1.5	6.0 6.0	ns	
$t_{PLH}$	Propagation Delay $\overline{LEBA}_n$ to $A_n$ or $\overline{LEAB}_n$ to $B_n$	1.5 1.5	6.5 6.5	1.5 1.5	7.5 7.5	ns	
$t_{PZL}$ $t_{PZH}$	Output Enable Time $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to $A_n$ or $B_n$ $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to $A_n$ or $B_n$	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns	
$t_{PLZ}$ $t_{PHZ}$	Output Disable Time $\overline{OEBA}_n$ or $\overline{OEAB}_n$ to $A_n$ or $B_n$ $\overline{CEBA}_n$ or $\overline{CEAB}_n$ to $A_n$ or $B_n$	1.5 1.5	6.5 6.5	1.5 1.5	7.0 7.0	ns	
$t_S$	Setup Time, HIGH or LOW, Data to $\overline{LEXx}_n$	2.5		2.5		ns	
$t_H$	Hold Time, HIGH or LOW, Data to $\overline{LEXx}_n$	1.5		1.5		ns	
$t_W$	Pulse Width, Latch Enable, LOW	3.0		3.0		ns	
$t_{OSHL}$ $t_{OSLH}$	Output to Output Skew (Note 3)		1.0 1.0			ns	

Note 3: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW ( $t_{OSHL}$ ) or LOW to HIGH ( $t_{OSLH}$ ). Parameter guaranteed by design.

## Dynamic Switching Characteristics

Symbol	Parameter	Conditions	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$	Units
				Typical	
$V_{OLP}$	Quiet Output Dynamic Peak $V_{OL}$	$C_L = 50 \text{ pF}$ , $V_{IH} = 3.3V$ , $V_{IL} = 0V$	3.3	0.8	V
$V_{OLV}$	Quiet Output Dynamic Valley $V_{OL}$	$C_L = 50 \text{ pF}$ , $V_{IH} = 3.3V$ , $V_{IL} = 0V$	3.3	0.8	V

## Capacitance

Symbol	Parameter	Conditions	Typical	Units
$C_{IN}$	Input Capacitance	$V_{CC} = \text{Open}$ , $V_I = 0V$ or $V_{CC}$	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{CC} = 3.3V$ , $V_I = 0V$ or $V_{CC}$	8	pF
$C_{PD}$	Power Dissipation Capacitance	$V_{CC} = 3.3V$ , $V_I = 0V$ or $V_{CC}$ , $F = 10 \text{ MHz}$	20	pF