Dual Synchronous Step-Down Controller For Low-Voltage Power Rails

FEATURES

- **High Efficiency, Low-Power Consumption**
- **D-Cap Mode Enables Fast Transient Response**
- **High Initial Reference Accuracy**
- **Low Output Ripple**
- **Wide Input Voltage Range: 4.5 V to 24 V**
- **Output Voltage Range: 0.76 V to 5.5 V**
- **Low-Side $R_{DS(on)}$ Loss-less Current Sensing**
- **Adaptive Gate Drivers with Integrated Boost Diode**
- **Internal 1.2-ms Voltage-Servo Soft Start**
- **Built-In 5-V Linear Regulator**

APPLICATIONS

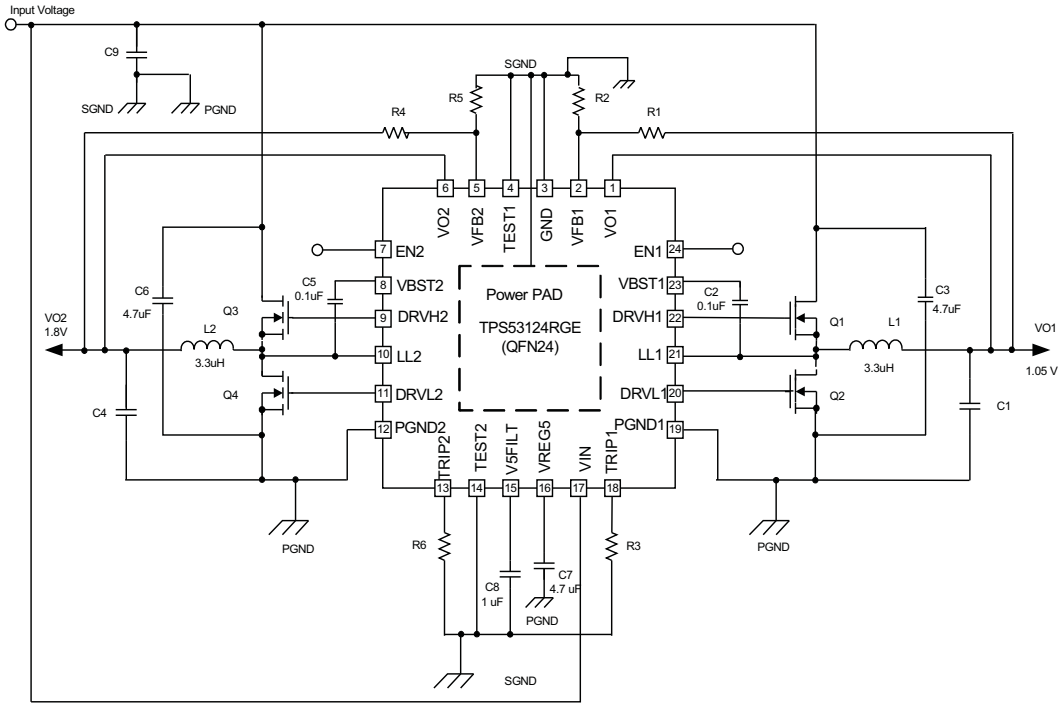
- **Digital TV Power Supply**
- **Networking Home Terminal**
- **Digital STB**

DESCRIPTION

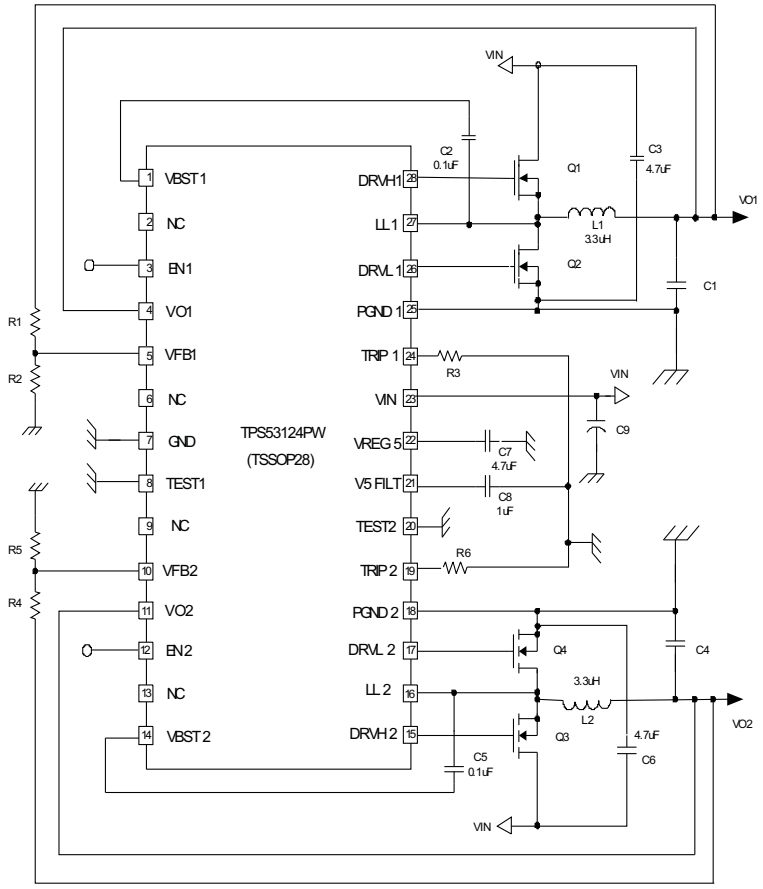
The TPS53124 is a dual, Adaptive on-time DCAP™ mode synchronous controller. The part enables system designers to cost effectively complete the suite of digital TV power bus regulators with the absolute lowest external component count and lowest standby consumption. The main control loop for the TPS53124 uses the D-CAP™ mode that optimized for low ESR output capacitors such as POSCAP or SP-CAP promises fast transient response with no external compensation. The part provides a convenient and efficient operation with conversion voltages from 4.5 V to 24 V and output voltage from 0.76 V to 5.5 V.

The TPS53124 is available in the 24-pin RGE package and in the 28-pin PW package and is specified from -40°C to 85°C ambient temperature range.

TYPICAL APPLICATION DIAGRAM



TSSOP-28 APPLICATION DIAGRAM



ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERING PART NUMBER	PINS	OUTPUT SUPPLY	ECO PLAN
-40°C to 85°C	Plastic quad	TPS53124RGET	24	Tape and Reel	Green (RoHS & no Sb/Br)
	Flat pack (QFN)	TPS53124RGER	24	Tape and Reel	
	TSSOP	TPS53124PWR	28	Tape and Reel	
	TSSOP	TPS53124PW	28	Tube	

(1) All packaging options have Cu NIPDAU lead/ball finish.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		VALUE	UNIT
Input Voltage Range	VIN,EN1,EN2	-0.3 to 26	V
	VBST1,VBST2	-0.3 to 32	
	VBST1,VBST2(wrt LLx)	-0.3 to 6	
	V5FILT,VFB1,VFB2,TRIP1,TRIP2,VO1,VO2, TEST1,TEST2	-0.3 to 6	
Output Voltage Range	DRVH1, DRVH2	-1 to 32	V
	DRVH1, DRVH2 (wrt LLx)	-0.3 to 6	
	LL1,LL2	-2 to 26	
	DRVL1,DRVL2,VREG5	-0.3 to 6	
	PGND1, PGND2	-0.3 to 0.3	
Operating ambient temperature range, T_A		-40 to 85	°C
Storage Temperature Range, T_{STG}		-55 to 150	
Junction Temperature Range, T_J		-40 to 150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

(2 oz. trace and copper pad with solder)

PACKAGE	T_A <25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
24-pin QFN	2.33 W	23.3 mW/°C	0.93 W
28-pin TSSOP	0.78 W	7.8 mW/°C	0.31 W

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
Supply Input Voltage Range	VIN	4.5	24	V
	V5FILT	4.5	5.5	
Input Voltage Range	VBST1, VBST2	-0.1	30	V
	VBST1, VBST2 (wrt LLx)	-0.1	5.5	
	VFB1,VFB2,VO1,VO2	-0.1	5.5	
	TRIP1,TRIP2	-0.1	0.3	
	EN1,EN2	-0.1	24	
Output Voltage Range	DRVH1,DRVH2	-0.1	30	V
	VBST1, VBST2 (wrt LLx)	-0.1	5.5	
	LL1,LL2	1.8	24	
	DRVL1,DRVL2, VREG5	-0.1	5.5	
	PGND1, PGND2	-0.1	0.1	
Operating Free-Air Temperature, T_A		-40	85	°C
Operating Junction Temperature, T_J		-40	125	

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, , VIN = 12 V, (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current						
I_{IN}	VIN supply current	VIN current, T_A = 25°C, VREG5 tied to V5FLT, EN1 = EN2 = 5 V, VFB1 = VFB2 = 0.8 V, LL1 = LL2 = 0.5 V		450	800	µA
I_{VINSDN}	VIN shutdown current	VIN current, T_A = 25°C, no load, EN1 = EN2 = 0 V			10	
VFB Voltage and Discharge Resistance						
V_{BG}	Bandgap initial regulation accuracy	T_A = 25°C	-1%		1%	
V_{VFBTH}	VFB threshold voltage	T_A = 25°C	755	765	775	mV
		T_A = -40°C to 85°C	752		778	
I_{VFB}	VFB input current	VFBx = 0.8 V, T_A = 25°C		-0.01	+/-0.1	µA
R_{DISCHG}	V_O discharge resistance	ENx = 0 V, VOx = 0.5 V,T_A = 25°C		40	80	Ω
VREG5 Output						
V_{VREG5}	VREG5 output voltage	T_A = 25°C ,5.5 V < VIN < 24 V, 0 < I_{VREG5} < 10 mA	4.8	5	5.2	V
V_{LN5}	Line regulation	5.5 V < VIN < 24 V, I_{VREG5} = 10 mA			20	mV
V_{LD5}	Load regulation	1 mA < I_{VREG5} < 10 mA			40	
I_{VREG5}	Output current	VIN = 5.5 V, VREG5 = 4.0 V, T_A = 25°C		170		mA
Output: N-Channel MOSFET Gate Drivers						
R_{DRVH}	DRVH resistance	Source, I_{DRVHx} = -100 mA		5.5	11	Ω
		Sink, I_{DRVHx} = 100 mA		2.5	5	
R_{DRVL}	DRVL resistance	Source, I_{DRVLx} = - 100 mA		4	8	Ω
		Sink, I_{DRVLx} = 100 mA		2	4	
T_D	Dead time	DRVHx-low to DRVLx-on	20	50	80	ns
		DRVLx-low to DRVHx-on	20	40	80	
Internal BST Diode						
V_{FBST}	Forward voltage	$V_{VREG5-VBSTx}$, I_F = 10 mA, T_A = 25°C	0.7	0.8	0.9	V
I_{VBSTLK}	VBST leakage current	VBST = 29 V, LL = 24 V, T_A = 25°C		0.1	1	µA
ON-Time Timer Control						
T_{ON1}	CH1 ON time	LL1 = 12 V, VO1 = 1.5 V		390		ns
T_{ON2}	CH2 ON time	LL2 = 12 V, VO2 = 1.05 V		210		
$T_{ON(min)}$	CH2 ON time	LL2 = 12 V, VO2 = 0.76 V		160		
$T_{OFF(min)}$	CH1/CH2 min OFF time	LL = 0.7 V T_A = 25°C, VFB = 0.7 V		390		
Soft Start						
T_{SS}	Internal SS time	Internal soft start VFB = 0.735 V	0.85	1.2	1.4	ms

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, , VIN = 12 V, (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
UVLO						
$V_{UV5VFILT}$	V5FILT UVLO threshold	Wake up	3.7	4	4.3	V
		Hysteresis	0.2	0.3	0.4	
LOGIC Threshold						
V_{ENH}	ENx H-level input voltage	EN 1/2	2			V
V_{ENL}	ENx L-level input voltage	EN 1/2			0.3	
Current Sense						
I_{TRIP}	TRIP source current	VTRIPx = 0.1 V, T_A = 25°C	8.5	10	11.5	µA
TC_{ITRIP}	I_{TRIP} temperature coefficient	On the basis of 25°C		4000		ppm/°C
$V_{OCL(off)}$	OCP compensation offset	($V_{TRIPx-GND}$ - $V_{PGNDx-LLx}$) voltage,$V_{TRIPx-GND}$ = 60 mV, T_A = 25°C	-10	0	10	mV
		($V_{TRIPx-GND}$ - $V_{PGNDx-LLx}$) voltage, $V_{TRIPx-GND}$ = 60 mV	-15		15	
$V_{R(trip)}$	Current limit threshold setting range	$V_{TRIPx-GND}$ voltage	30		200	
Output Undervoltage and Overvoltage Protection						
V_{OVP}	Output OVP trip threshold	OVP detect	110%	115%	120%	
T_{OVPDEL}	Output OVP prop delay			1.5		µs
V_{UVP}	Output UVP trip threshold	UVP detect	65%	70%	75%	
		Hysteresis (recovery < 20 µs)		10%		
T_{UVPDEL}	Output UVP delay		17	30	40	µs
T_{UVPEN}	Output UVP enable delay		1.2	2	2.5	ms
Thermal Shutdown						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature(1)		150		°C
		Hysteresis(1)		20		

(1) Ensured by design. Not production tested.

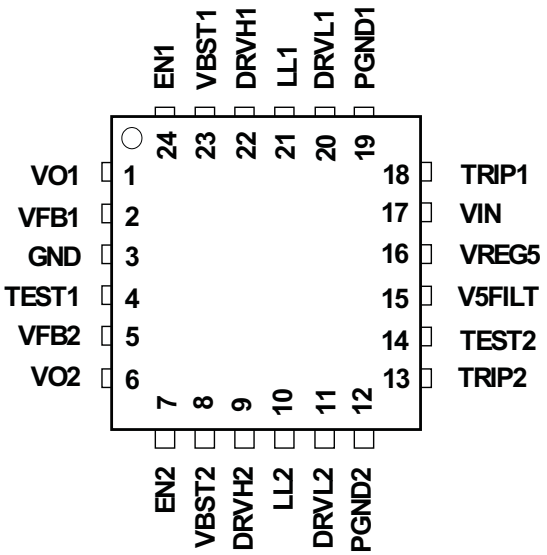
DEVICE INFORMATION

TERMINAL FUNCTIONS

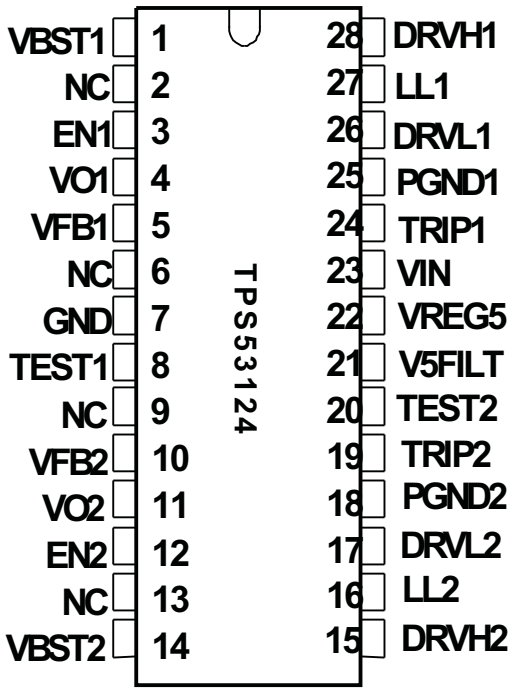
TERMINAL			I/O	DESCRIPTION
NAME	GFN24	TSSOP28		
VBST1, VBST2	23, 8	1, 14	I	Supply input for high-side NFET driver (boost terminal). Connect capacitor from this pin to respective LL terminals. An internal PN diode is connected between VREG5 to each of these pins. User can add external schottky diode if forward drop is critical to drive the NFET.
EN1, EN2	24, 7	3, 12	I	Channel 1 and Channel 2 enable pins.
VO1, VO2	1, 6	4, 11	I	Output connections to SMPS. These terminals serve ON-time adjustment, output discharge.
VFB1, VFB2	2, 5	5, 10	I	SMPS feedback inputs. Connect with feedback resistor divider.
GND	3	7	I	Signal ground pin.
DRVH1, DRVH2	22, 9	28, 15	O	High-side NFET driver outputs. LL referenced floating drivers. The gate drive voltage is defined by the voltage across VBST to LL node flying capacitor.
LL1, LL2	21, 10	27, 16	I/O	Switch-node connections for high-side drivers. Also serve as input to current comparators.
DRVL1, DRVL2	20, 11	26, 17	O	Synchronous NFET driver outputs. PGND referenced drivers. The gate drive voltage is defined by VREG5 voltage.
PGND1, PGND2	19, 12	25, 18	I/O	Ground returns for DRVL1 and DRVL2. Also serve as input of current comparators. Connect PGND1, PGND2 and GND strongly together near the device.
TRIP1, TRIP2	18, 13	24, 19	I	Over-current trip point set input. Connect resistor from this pin to GND to set threshold for synchronous $R_{DS(on)}$ sense. Voltage across this pin and GND is compared to voltage across PGND and LL at over current comparator.
VIN	17	23	I	Supply Input for 5-V linear regulator.
V5FILT	15	21	I	5-V supply input for the entire control circuit except the NFET drivers. Connect capacitor (typical 1 μF) from GND to V5FILT. V5FILT is connected to VREG5 via internal resistor.
VREG5	16	20	O	5-V power supply output. VREG5 is connected to V5FILT via internal resistor.
TEST1, TEST2	4, 14	8, 20	I/O	Used for test only. Pin should be connected to GND

Pinout Diagrams

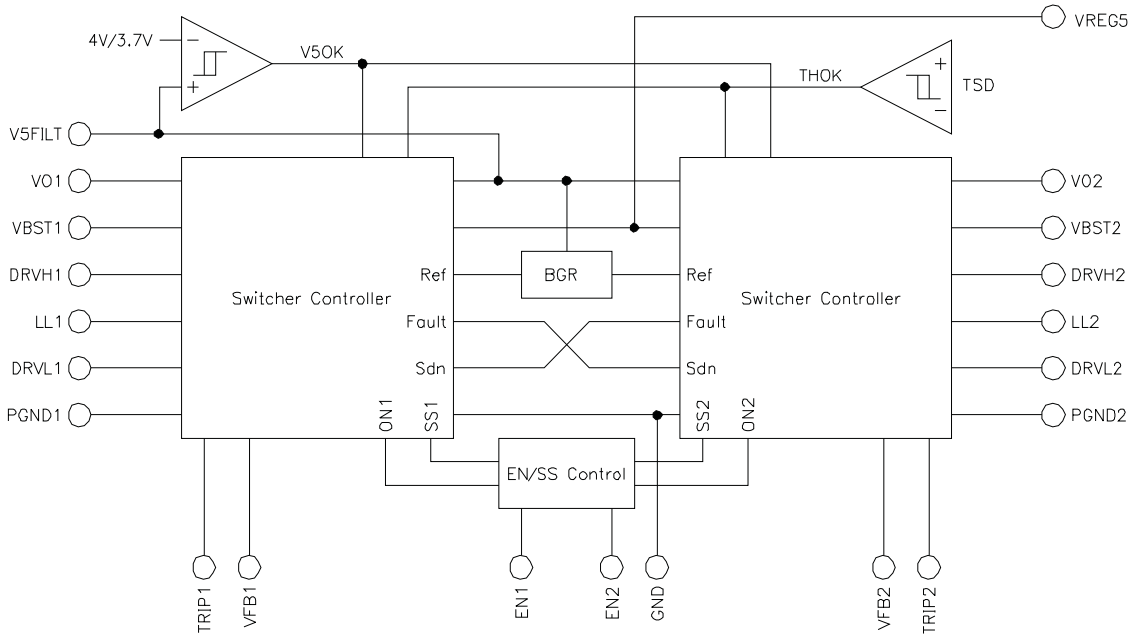
QFN Package (Top View)

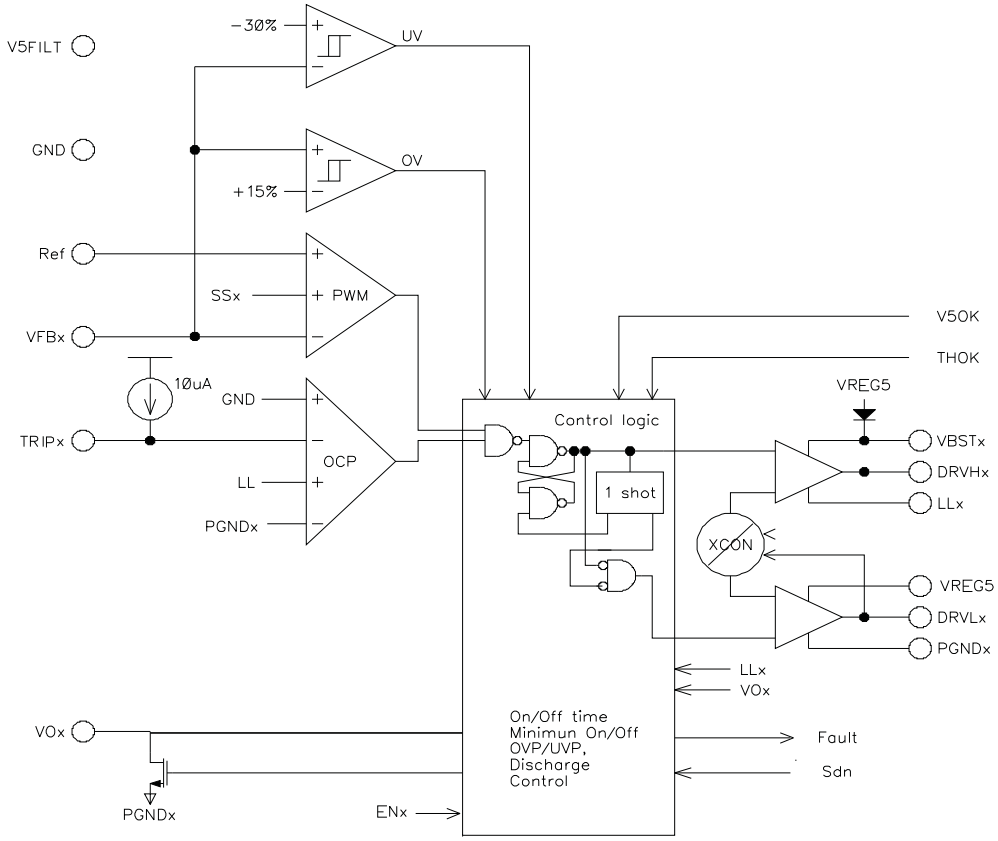


TSSOP Package (Top View)



Functional Block Diagram





DETAILED DESCRIPTION

PWM Operation

The main control loop of the switching mode power supply (SMPS) is designed as an adaptive on-time pulse width modulation (PWM) controller. It supports a proprietary D-CAP™ Mode. D-CAP™ Mode uses internal compensation circuit and is suitable for low external component count configuration with appropriate amount of ESR at the output capacitor(s). The output ripple bottom voltage is monitored at a feedback point voltage.

At the beginning of each cycle, the synchronous high-side MOSFET is turned on, or becomes ON state. This MOSFET is turned off, or becomes OFF state, after internal one-shot timer expires. This one shot is determined by the converter's input voltage ,VIN, and the output voltage ,VOUT, to keep frequency fairly constant over the input voltage range, hence it is called adaptive on-time control. The high-side MOSFET is turned on again when feedback information indicates insufficient output voltage. Repeating operation in this manner, the controller regulates the output voltage.

Low-Side Driver

The low-side driver is designed to drive high current low $R_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistance. A dead time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on. 5-V bias voltage is delivered from internal regulator VREG5 output. The instantaneous drive current is supplied by an input capacitor connected between VREG5 and GND. The average drive current is equal to the gate charge at V_{GS} = 5 V times switching frequency. This gate drive current as well as the high-side gate drive current times 5 V makes the driving power which need to be dissipated from TPS53124 package.

High-Side Driver

The high-side driver is designed to drive high current, low $R_{DS(on)}$ N-channel MOSFET(s). When configured as a floating driver, 5-V bias voltage is delivered from VREG5 supply. The average drive current is also calculated by the gate charge at V_{GS} = 5 V times switching frequency. The instantaneous drive current is supplied by the flying capacitor between VBSTx and LLx pins. The drive capability is represented by its internal resistance.

PWM Frequency and Adaptive On-Time Control

TPS53124 employs adaptive on-time control scheme and does not have a dedicated oscillator on board. However, the part runs with pseudo-constant frequency by feed-forwarding the input and output voltage into the on-time one-shot timer. The on-time is controlled inverse proportional to the input voltage and proportional to the output voltage so that the duty ratio will be kept as VOUT/VIN technically with the same cycle time.

Soft Start

The TPS53124 has an internal, 1.2 ms, voltage servo softstart for each channel. When the ENx pin becomes high, an internal DAC begins ramping up the reference voltage to the PWM comparator. Smooth control of the output voltage is maintained during start up. As TPS53124 shares one DAC with both channels, if ENx pin is set to high while another channel is starting up, soft start is postponed until another channel soft start has completed. If both of EN1 and EN2 are set high at a same time, both channels start up at same time.

Output Discharge Control

TPS53124 discharges the output when ENx is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO, and thermal shutdown). TPS53124 discharges outputs using an internal 40-Ω MOSFET which is connected to VOx and PGNDx. The external low-side MOSFET is not turned on for the output discharge operation to avoid the possibility of causing negative voltage at the output.

This discharge ensures that, on start, the regulated voltage always start from zero volts.

Current Protection

TPS53124 has cycle-by-cycle over current limiting control. The inductor current is monitored during the 'OFF' state and the controller keeps the OFF state during the inductor current is larger than the over-current trip level. In order to provide both good accuracy and cost effective solution, TPS53124 supports temperature compensated MOSFET $R_{DS(on)}$ sensing. TRIPx pin should be connected to GND through the trip voltage setting resistor, R_{TRIP}. TRIPx terminal sources 10-µA I_{TRIP} current at the ambient temperature and the trip level is set to the OCL trip voltage V_{TRIP} as below:

$$V_{TRIP}(mV) = R_{TRIP}(k\Omega) \times 10(\mu A) \quad (1)$$

The trip level should be in the range of 30 mV to 200 mV over all operational temperature. The inductor current is monitored by the voltage between PGNDx pin and LLx pin. I_{TRIP} has 4000ppm/°C temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. PGNDx is used as the positive current sensing node so that PGNDx should be connected to the source terminal of the bottom MOSFET.

As the comparison is done during the OFF state, V_{TRIP} sets valley level of the inductor current. Thus, the load current at over-current threshold, I_{OCP}, can be calculated as follows:

$$I_{OCP} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{I_{RIPPLE}}{2} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

In an over-current condition, the current to the load exceeds the current to the output capacitor; thus the output voltage tends to fall off. Eventually, it will end up with crossing the under voltage protection threshold and shutdown.

Over/Under Voltage Protection

TPS53124 monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes higher than 115% of the target voltage, the OVP comparator output goes high and the circuit latches as the high-side MOSFET driver OFF and the low-side MOSFET driver ON.

When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 30 µs, TPS53124 latches OFF both top and bottom MOSFET drivers, and shut off both drivers of another channel. This function is enabled approximately 2.0 ms.

UVLO Protection

TPS53124 has V5FILT Under Voltage Lock Out protection (UVLO). When the V5FILT voltage is lower than UVLO threshold voltage TPS53124 is shut off. This is non-latch protection.

Thermal Shutdown

TPS53124 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 150°C), the switchers will be shut off as both DRVH and DRVL at low, the output discharge function enabled. Then TPS53124 is shut off. This is non-latch protection.

Typical Characteristics

VIN SUPPLY CURRENT vs JUNCTION TEMPERATURE

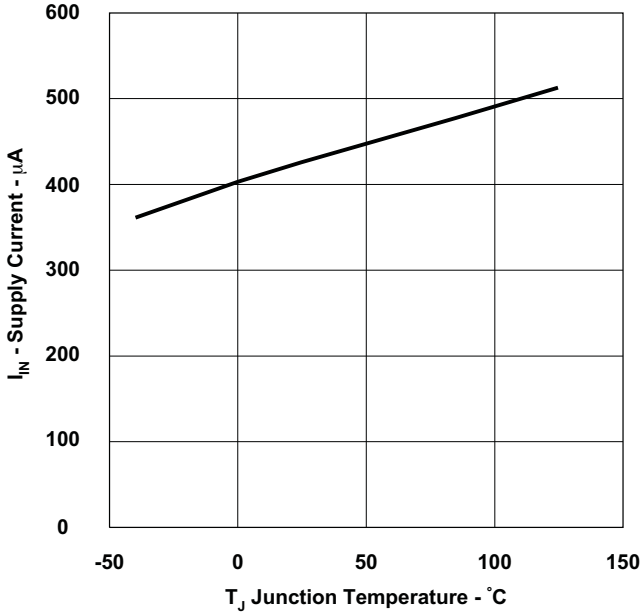


Figure 1.

VIN SHUTDOWN CURRENT vs JUNCTION TEMPERATURE

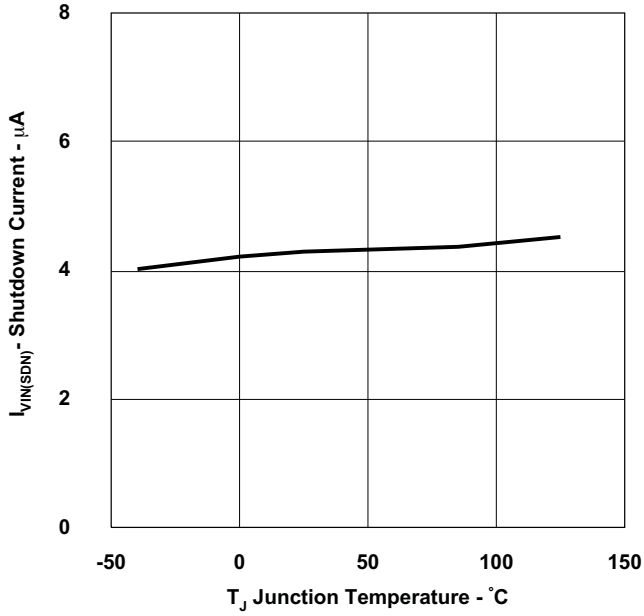


Figure 2.

ITRIP SOURCE CURRENT vs JUNCTION TEMPERATURE

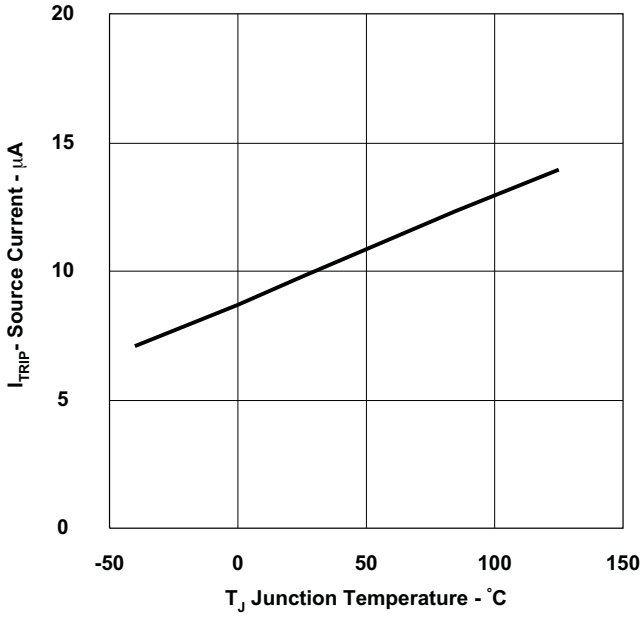


Figure 3.

SWITCHING FREQUENCY I_O = 1A vs JUNCTION TEMPERATURE

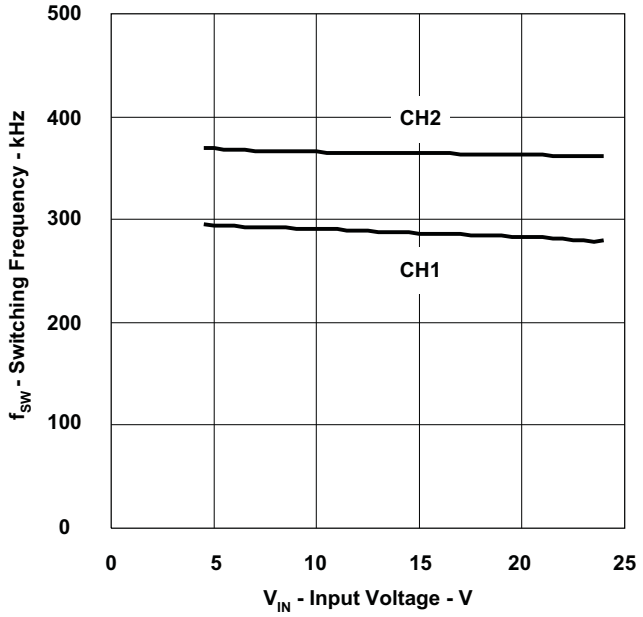


Figure 4.

Typical Characteristics (continued)

SWITCHING FREQUENCY I_O = 1A vs OUTPUT CURRENT

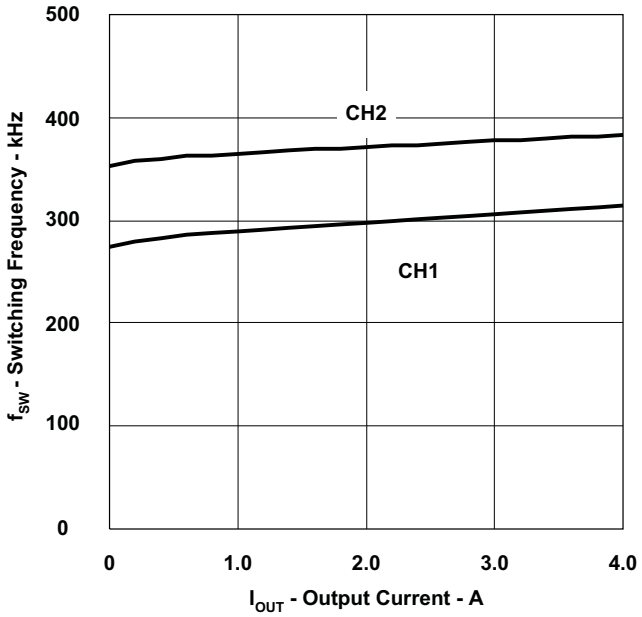


Figure 5.

1.05-V OUTPUT VOLTAGE vs OUTPUT CURRENT

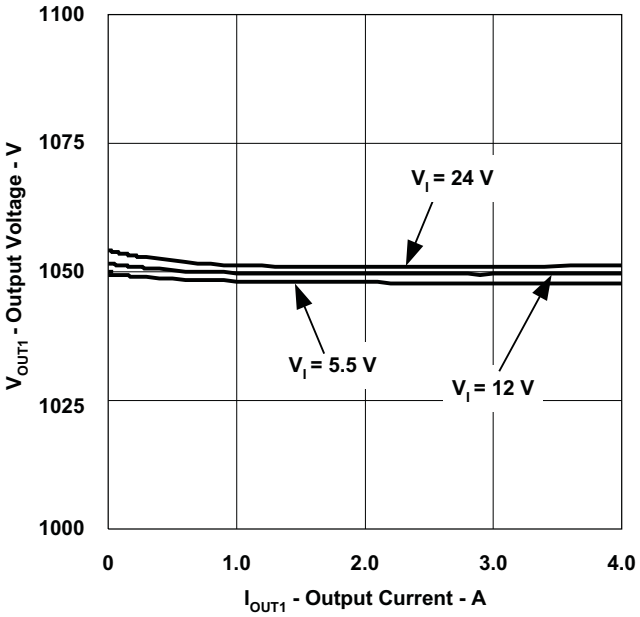


Figure 6.

1.8-V OUTPUT VOLTAGE vs OUTPUT CURRENT

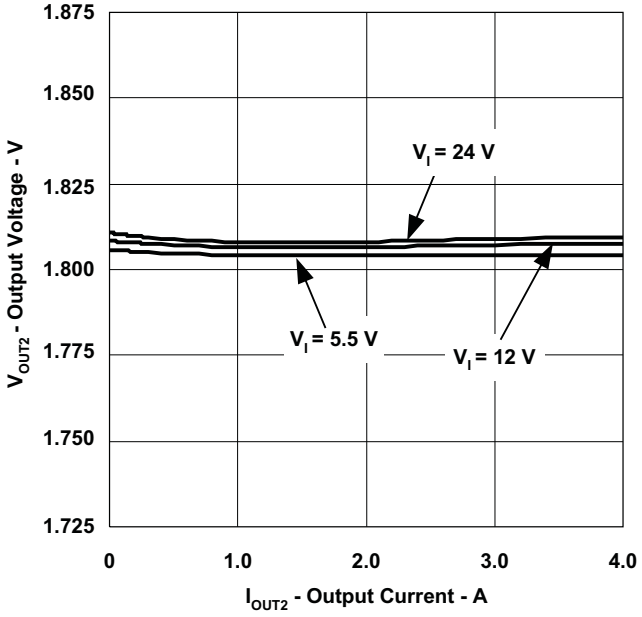


Figure 7.

1.05-V OUTPUT VOLTAGE vs INPUT VOLTAGE

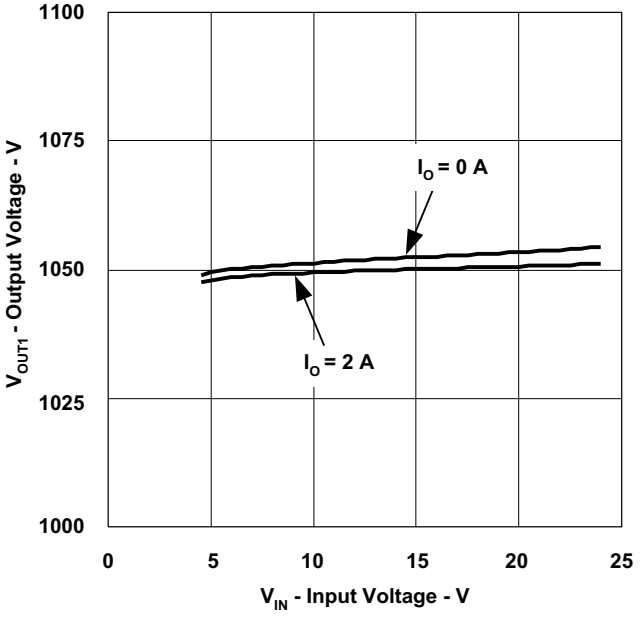


Figure 8.

Typical Characteristics (continued)

1.8-V OUTPUT VOLTAGE vs INPUT VOLTAGE

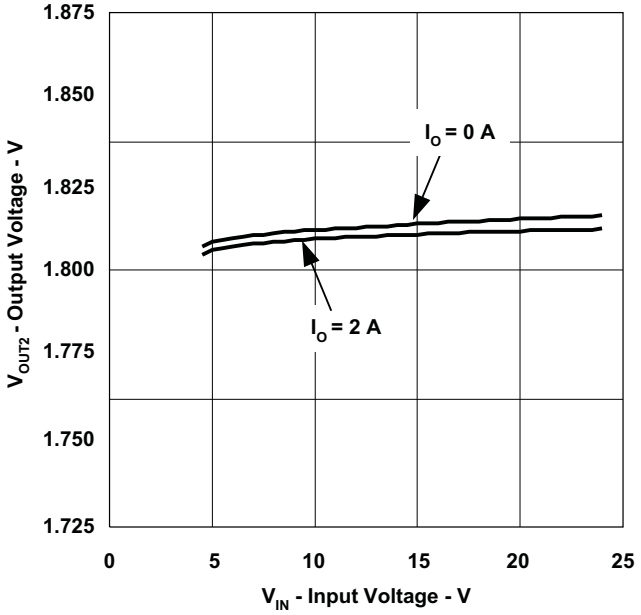


Figure 9.

1.8-V LOAD TRANSIENT RESPONSE

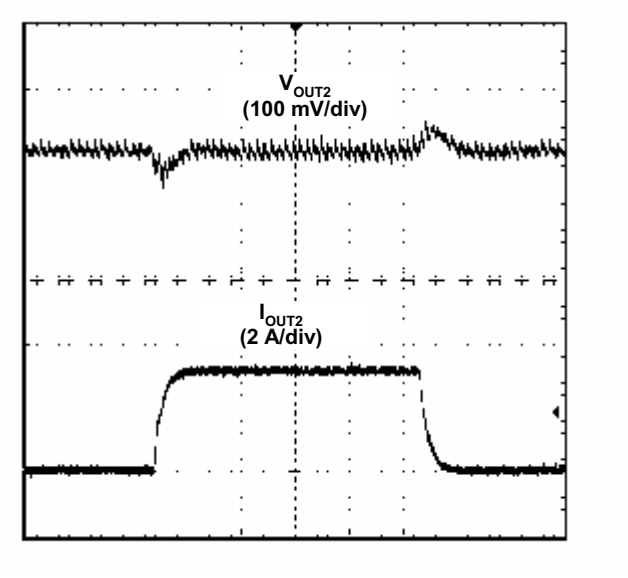


Figure 10.

1.05-V LOAD TRANSIENT RESPONSE

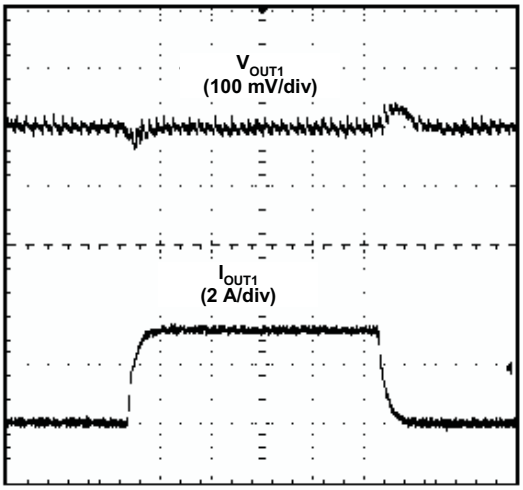


Figure 11.

APPLICATION INFORMATION

Loop Compensation and External Parts Selection

A buck converter system using D-CAP™ Mode can be simplified as below.

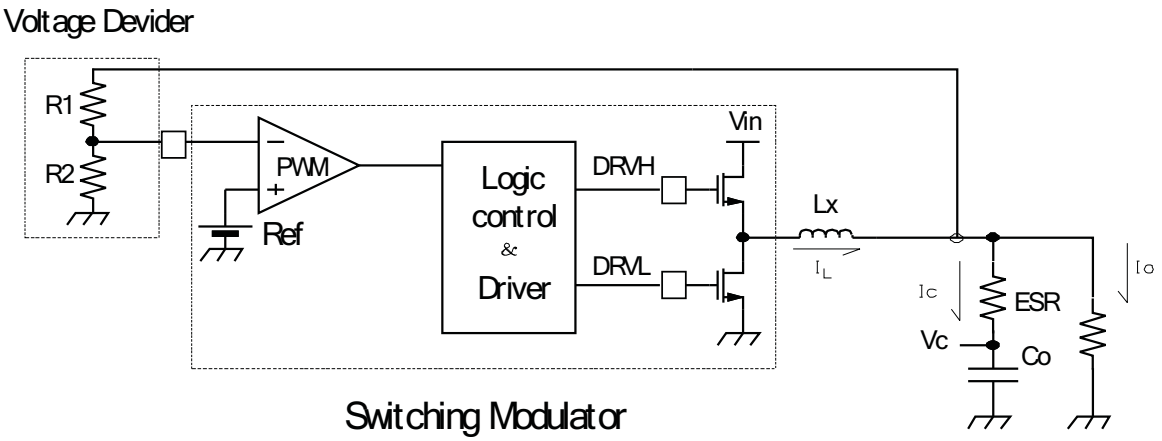


Figure 12. Simplifying the Modulator

The output voltage is compared with internal reference voltage after divider resistors,R1 and R2. The PWM comparator determines the timing to turn on top MOSFET. The gain and speed of the comparator is high enough to keep the voltage at the beginning of each on cycle (or the end of off cycle) substantially constant. The dc output voltage may have line regulation due to ripple amplitude that slightly increases as the input voltage increase.

For the loop stability, the 0dB frequency, f_0, defined below need to be lower than 1/3 of the switching frequency.

$$f_O = \frac{1}{2\pi \times ESR \times C_O} \leq \frac{f_{SW}}{3} \tag{3}$$

Although D-CAP™ Mode provides many advantages such as ease-of-use, minimum external components configuration and extremely short response time, a sufficient amount of feedback signal needs to be provided by external circuit to reduce jitter level. This is due to not employing an error amplifier in the loop. The required signal level is approximately 10 mV at the comparing point(VFB terminal). This gives Vripples at the output node becomes Equation 4. The output capacitor's ESR should meet this requirement.

$$V_{RIPPLE} = \frac{V_{OUT}}{V_{FBx}} \times 10 \left[mV \right] \tag{4}$$

The external components selection is much simpler in D-CAP™ Mode.

1. Choose inductor.

   The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current. Larger ripple current increases output ripple voltage, improves S/N ratio and contributes to a stable operation.

$$L = \frac{1}{I_{IND(ripple)} \times f} \cdot \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} = \frac{3}{I_{OUT(max)} \times f} \times \frac{\left(V_{IN(max)} - V_{OUT}\right) \times V_{OUT}}{V_{IN(max)}} \quad (5)$$

   The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated as follows.

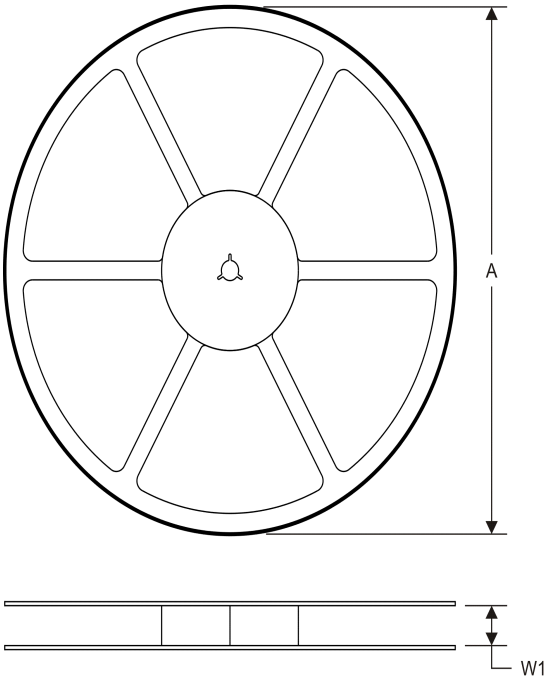
$$I_{IND(peak)} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{L \times f} \times \frac{(V_{IN(max)} - V_{OUT}) \times V_{OUT}}{V_{IN(max)}} \quad (6)$$

2. Choose output capacitor.

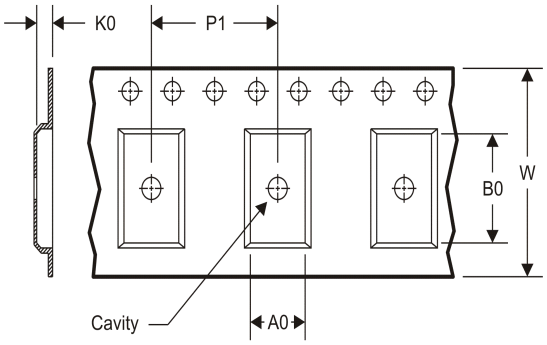
   Polymer aluminum capacitor, organic semiconductor capacitor or specialty polymer capacitor are recommended. Determine ESR to meet required ripple voltage indicated previously.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



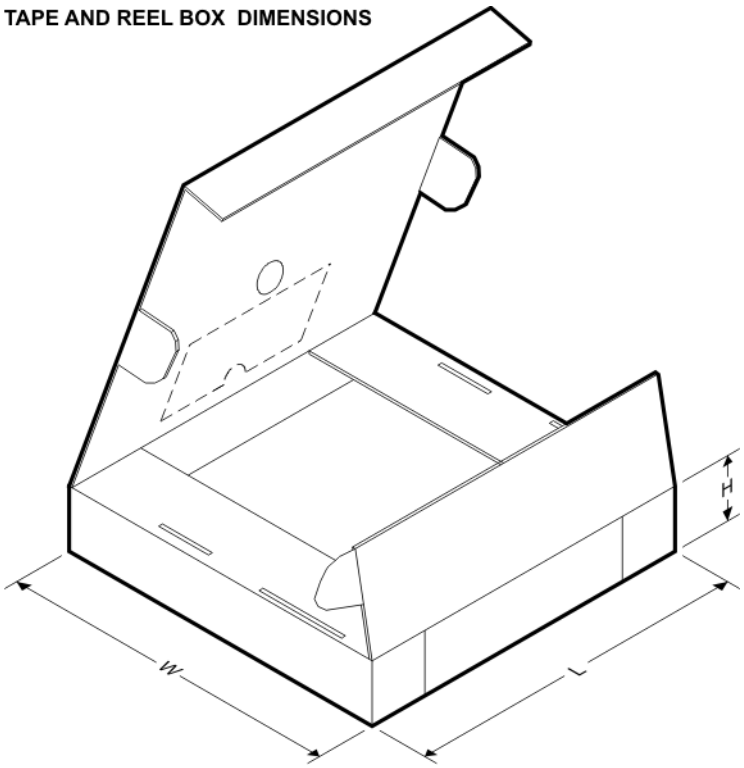
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53124PWR	TSSOP	PW	28	2000	330.0	16.4	7.1	10.4	1.6	12.0	16.0	Q1
TPS53124RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS53124RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS53124RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS53124RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

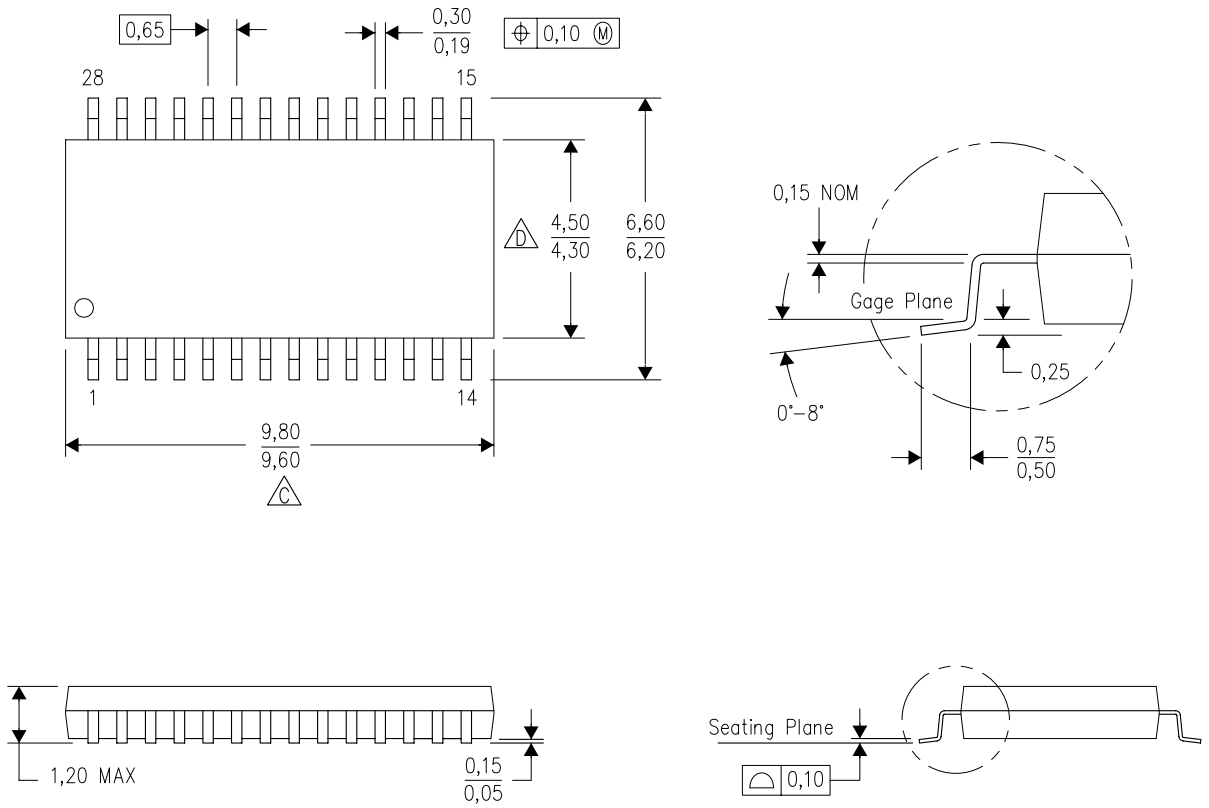
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53124PWR	TSSOP	PW	28	2000	367.0	367.0	38.0
TPS53124RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS53124RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS53124RGET	VQFN	RGE	24	250	210.0	185.0	35.0
TPS53124RGET	VQFN	RGE	24	250	210.0	185.0	35.0

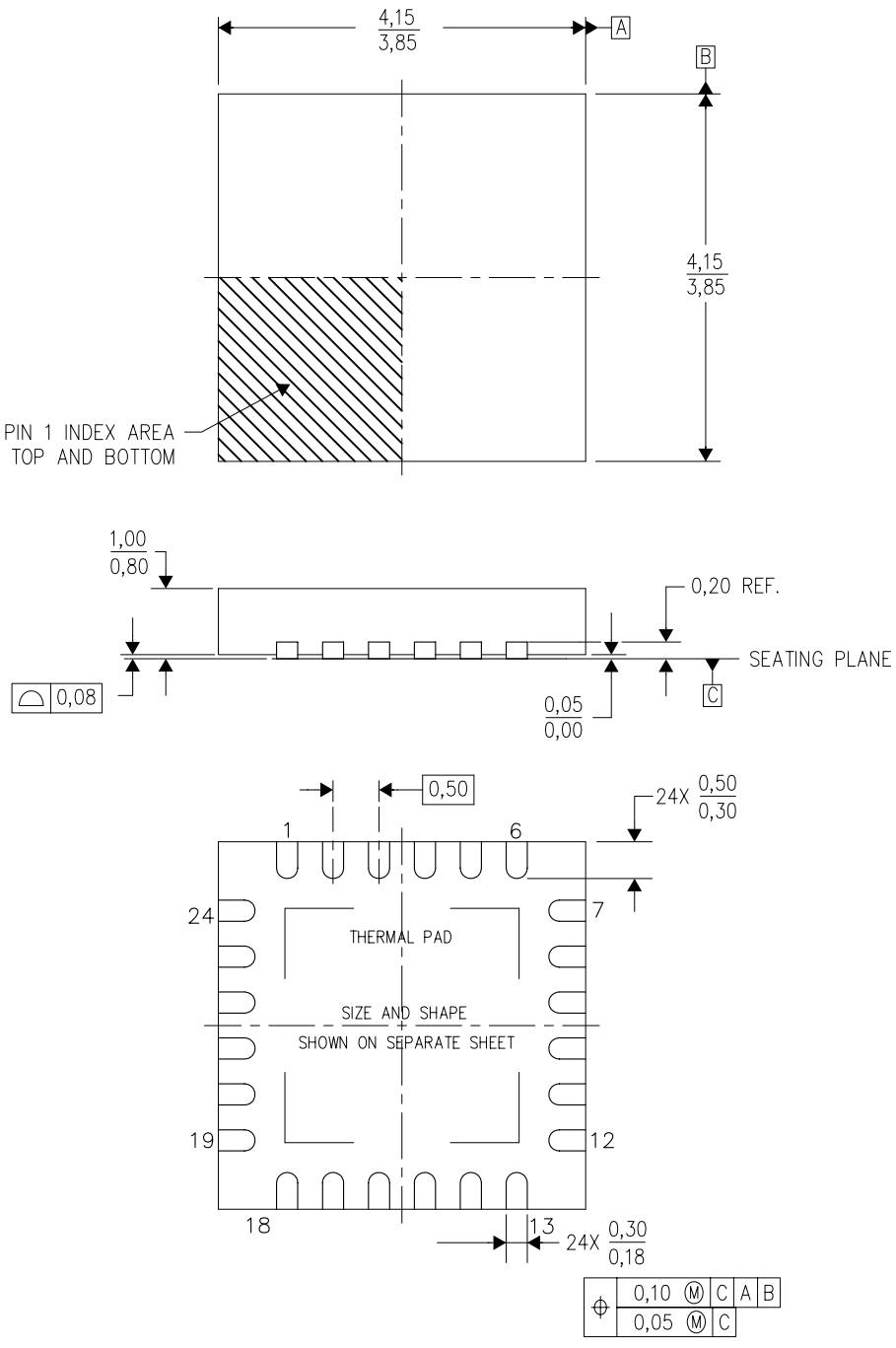
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

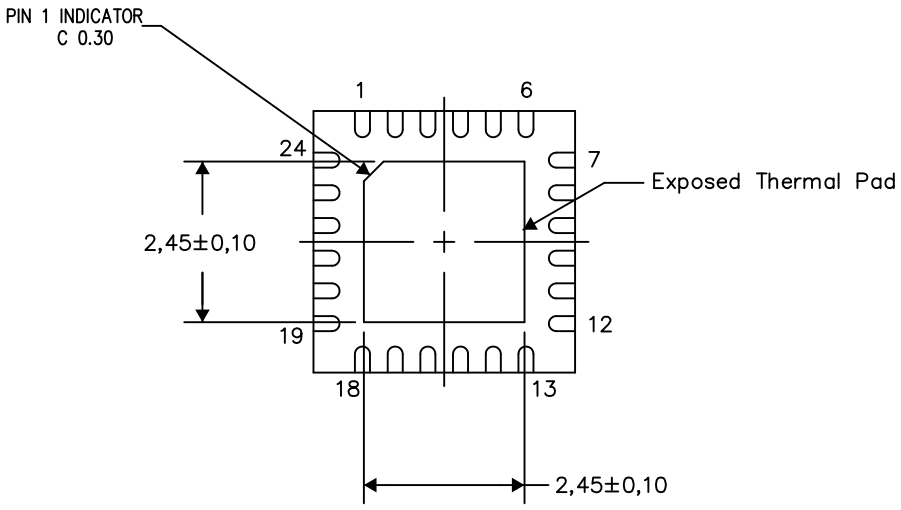
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



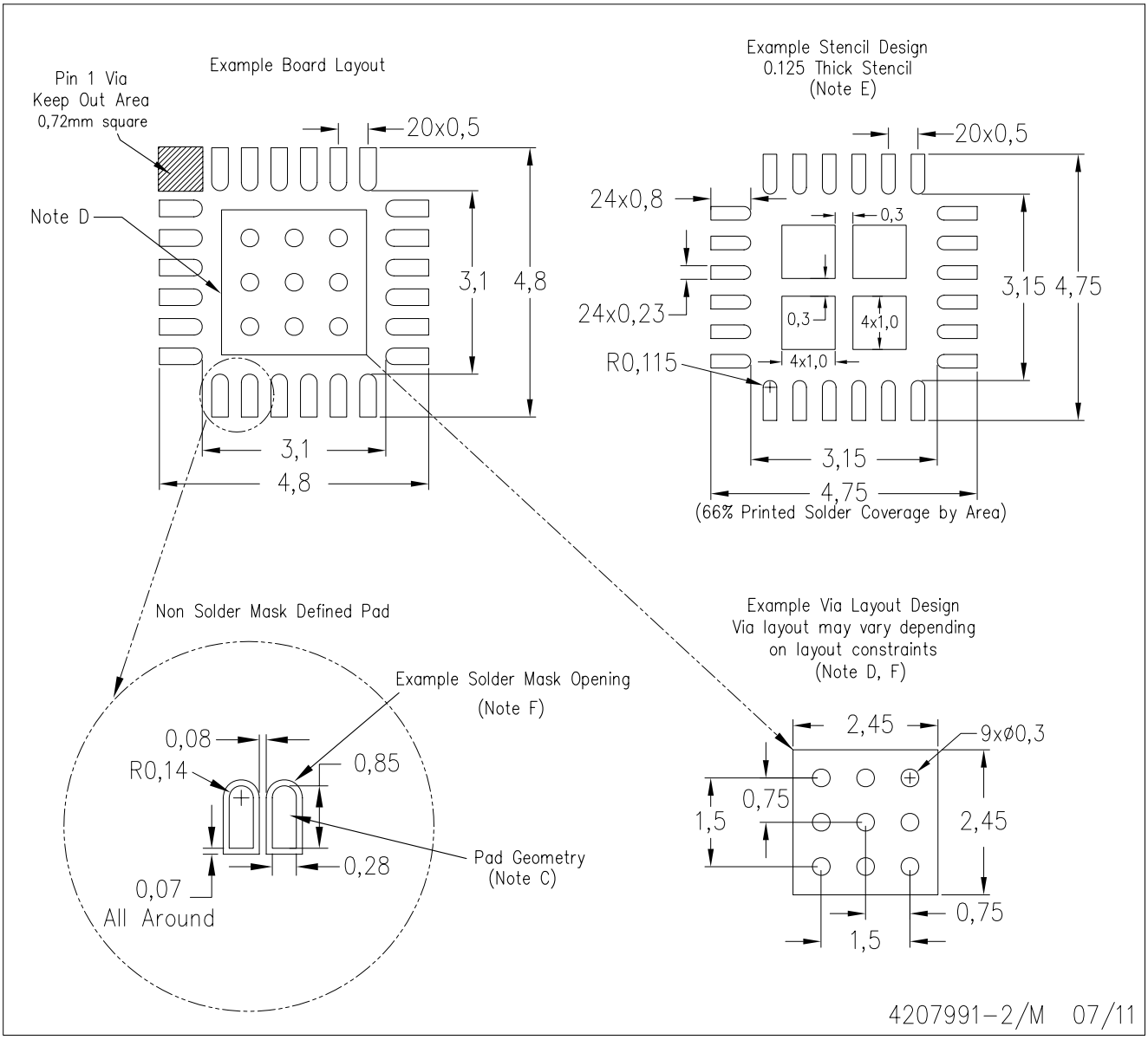
Bottom View

Exposed Thermal Pad Dimensions

4206344–3/AA 04/12

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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