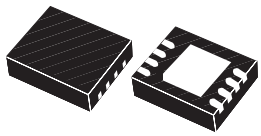
L6747C

High current MOSFET driver

Features

- Dual MOSFET driver for synchronous rectified converters
- High driving current for fast external MOSFET switching
- High frequency operation
- Enable pin
- Adaptive dead-time management
- Flexible gate-drive: 5 V to 12 V compatible
- High-impedance (HiZ) management for output stage shutdown
- Preliminary overvoltage (OV) protection
- VFDFPN8 3x3 mm package



VFDFPN8 3x3 mm

Applications

- High current VRM / VRD for desktop / server / workstation CPUs
- High current and high efficiency DC-DC converters

Description

The L6747C is a flexible, high-frequency dual-driver specifically designed to drive N-channel MOSFETs connected in synchronous-rectified buck topology.

Combined with ST PWM controllers, the driver allows the implementation of complete voltage regulator solutions for modern high-current CPUs and for DC-DC conversion in general.

The L6747C embeds high-current drivers for both high-side and low-side MOSFETS. The device accepts a flexible power supply of 5 V to 12 V. This allows optimization of the high-side and low-side gate-drive voltage to maximize system efficiency.

Anti shoot-through management prevents the high-side and low-side MOSFETs from conducting simultaneously and, combined with adaptive dead-time control, minimizes the LS body diode conduction time.

The L6747C features preliminary OV protection to protect the load from dangerous overvoltage due to MOSFET failures at startup.

The driver is available in a VFDFPN8 3x3 mm package.

Table 1. Device summary

Order codes	Package	Packing
L6747C	VFDFPN8	Tube
L6747CTR	VFDFPN8	Tape and reel

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1 Typical application circuit and block diagram

Figure 1. L6747C typical application circuit

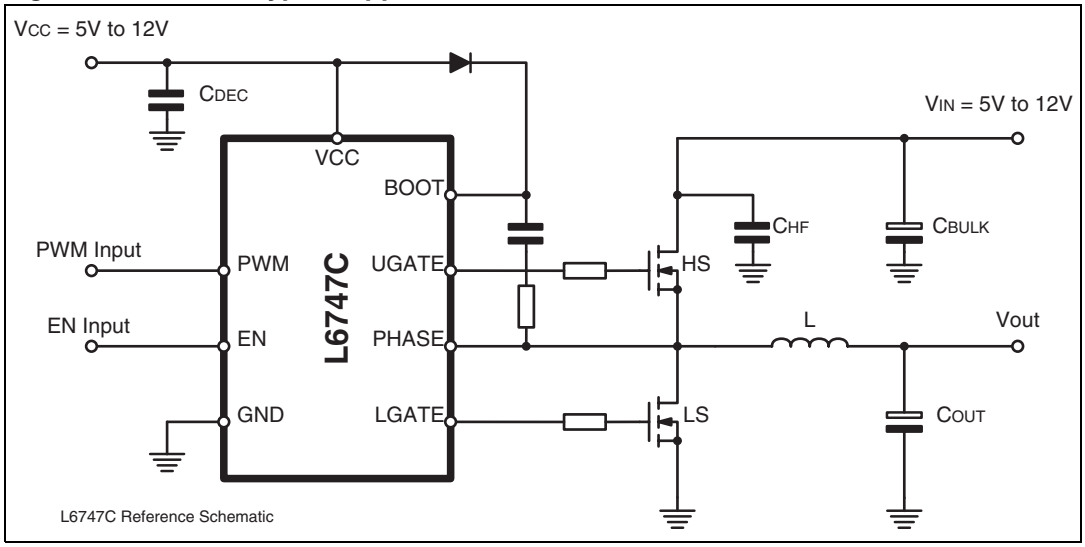
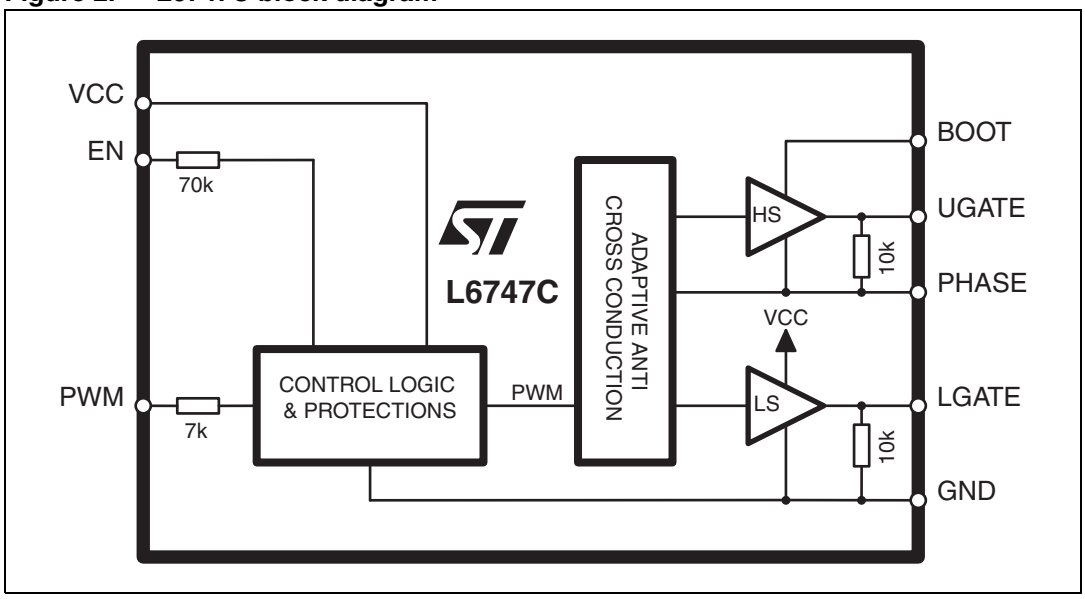


Figure 2. L6747C block diagram



2 Pin information and thermal data

2.1 Pin information

Figure 3. Pin connection diagram (top view)

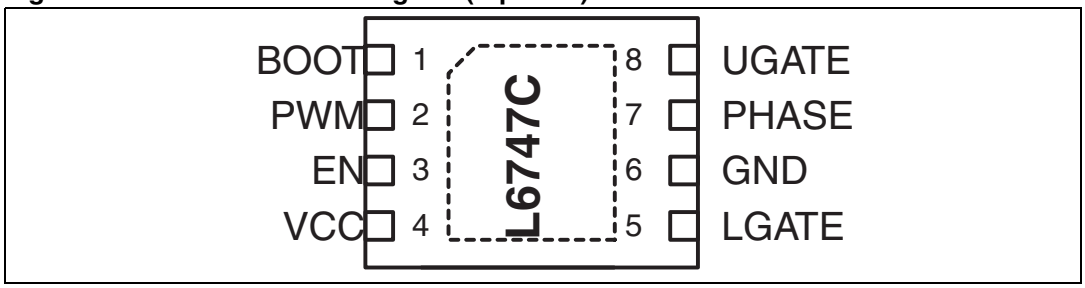


Table 2. Pin descriptions

Pin #	Name	Function
1	BOOT	High-side driver supply. This pin supplies the high-side floating driver. Connect through a R_{BOOT} - C_{BOOT} (2.2Ω - 220nF typ.) network to the PHASE pin. See *Section 4.3* for guidance in designing the capacitor value.
2	PWM	Control input for the driver; 5V compatible, internally clamp to 3.3V. This pin controls the state of the driver and which external MOSFET must be turned ON according to EN status. If manages the high-impedance (HiZ) state which sets all the MOSFETs to OFF if externally set in the HiZ window (See *Table 5*). See *Section 4.1* for details of HiZ.
3	EN	Enable input for the driver; 5V compatible, internally clamp to 3.3V. Pull high to enable the driver based on the PWM status. Pull low to enter HiZ state with all MOSFET OFF, regardless of the PWM status. See *Section 4.1* for details of HiZ.
4	VCC	Device and LS driver power supply. Connect to any voltage between 5V and 12V. Bypass with low-ESR MLCC capacitor to GND (1μF typ).
5	LGATE	Low-side driver output. Connect directly to the low-side MOSFET gate. A small series resistor may be used to reduce dissipated power especially in high frequency applications.
6	GND	All internal references, logic and drivers are referenced to this pin. Connect to the PCB ground plane.
7	PHASE	High-side driver return path. Connect to the high-side MOSFET source. This pin is also monitored for adaptive dead-time management and pre-OV protection. Internal clamp circuitry prevent leakage from this pin in disable conditions.

Table 2. Pin descriptions (continued)

Pin #	Name	Function
8	UGATE	High-side driver output. Connect to high-side MOSFET gate. A small series resistor may be used to control the PHASE pin negative spike.
-	TH. PAD	Thermal pad connects the silicon substrate and makes good thermal contact with the PCB. Connect to the PGND plane.

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal resistance junction-to-ambient (device soldered on 2s2p, 67mm x 69mm board)	45	°C/W
R_{THJC}	Thermal resistance junction-to-case	5	°C/W
T_{MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature range	0 to 150	°C
T_J	Junction temperature range	0 to 125	°C
P_{TOT}	Maximum power dissipation at 25°C (device soldered on 2s2p,67mm x 69mm board)	2.25	W

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	to GND	-0.3 to 20	V
V_{BOOT}	to GND to GND, t < 200 ns to PHASE	-0.3 to 41 -0.3 to 44 -0.3 to 15	V
V_{UGATE}	t < 200 ns	PHASE -0.3 to BOOT +0.3 PHASE -1 to BOOT +0.3	V
V_{PHASE}	to GND to GND; t < 200 ns, VCC = 12V	-8 to 26 -8 to 30	V
V_{LGATE}	to GND to GND, t < 200 ns	-0.3 to VCC + 0.3 -1.5 to VCC + 0.3	V
V_{PWM}, V_{EN}	to GND	-0.3 to 7	V

3.2 Electrical characteristics

V_{CC} = 12 V±15%, T_J = 0 °C to 70 °C unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current and power-on						
I_{CC}	VCC supply current	UGATE = LGATE = OPEN; BOOT = 12V; EN = 1; PWM = 1		1.5	2.0	mA
		UGATE = LGATE = OPEN; BOOT = 12V; EN = 1; PWM = 0		2.7	3.5	mA
		UGATE = LGATE = OPEN; BOOT = 12V; EN = 0		1.0	1.5	mA
I_{BOOT}	BOOT supply current	UGATE = OPEN; PHASE = GND; BOOT = 12V; EN = 1; PWM = 1		2.3	3.3	mA
		UGATE = OPEN; PHASE = GND; BOOT = 12V; EN = 1; PWM = 0		2.0	3.0	mA
		UGATE = OPEN; PHASE = GND; BOOT = 12V; EN = 0		1.3	2.3	mA
$UVLO_{VCC}$	VCC turn-ON	VCC rising			4.1	V
	VCC turn-OFF	VCC falling	3.5			V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
PWM and EN INPUT						
PWM	Input high - V_{PWM_IH}	PWM rising	2			V
	Input low - V_{PWM_IL}	PWM falling			0.8	V
	Input leakage	PWM = GND	-5		5	µA
t_{HiZ}	HiZ hold-off time	See *Figure 4*		120		ns
t_{prop_L}	Propagation delays	See *Figure 4*		25	35	ns
t_{prop_H}				30	45	ns
EN	Input High - V_{EN_IH}	EN rising	2			V
	Input Low - V_{EN_IH}	EN falling			0.8	V
Gate drivers						
R_{HIHS}	HS source resistance	BOOT - PHASE = 12V; 100mA		1.4	2.0	Ω
I_{UGATE}	HS source current (1)	BOOT - PHASE = 12V; C_{UGATE} to PHASE = 3.3nF		3.5		A
R_{LOHS}	HS sink resistance	BOOT - PHASE = 12V; 100mA		1.0	1.5	Ω
R_{HILS}	LS source resistance	100mA		1.4	2.0	Ω
I_{LGATE}	LS source current (1)	C_{LGATE} to GND = 5.6nF		3.5		A
R_{LOLS}	LS sink resistance	100mA		1.0	1.5	Ω
Protections						
V_{PRE_OV}	Pre-OV threshold	PHASE rising	1.7	1.8		V

1. Parameter(s) guaranteed by design, not fully tested in production

4 Device description and operation

The L6747C provides high-current driving control for both high-side and low-side N-channel MOSFETs, connected as step-down DC-DC converters and driven by an external PWM signal. The integrated high-current drivers allow the use of different types of power MOSFETs (also multiple MOS to reduce the equivalent $R_{DS(on)}$), maintaining fast switching transition. The driver for the high-side MOSFET uses the BOOT pin for supply and the PHASE pin for return. The driver for the low-side MOSFET uses the VCC pin for supply and the PGND pin for return.

The driver includes anti-shoot-through and adaptive dead-time control to minimize low-side body diode conduction time, maintaining good efficiency and eliminating the need for Schottky diodes. When the high-side MOSFET turns off, the voltage on its source begins to fall; when the voltage falls below the proper threshold, the low-side MOSFET gate drive voltage is suddenly applied. When the low-side MOSFET turns off, the voltage at the LGATE pin is sensed. When it drops below the proper threshold, the high-side MOSFET gate drive voltage is suddenly applied. If the current flowing in the inductor is negative, the source of the high-side MOSFET never drops. To allow the low-side MOSFET to turn on even in this case, a watchdog controller is enabled. If the source of the high-side MOSFET does not drop, the low-side MOSFET is switched on, allowing the negative current of the inductor to recirculate. This mechanism allows the system to regulate even if the current is negative.

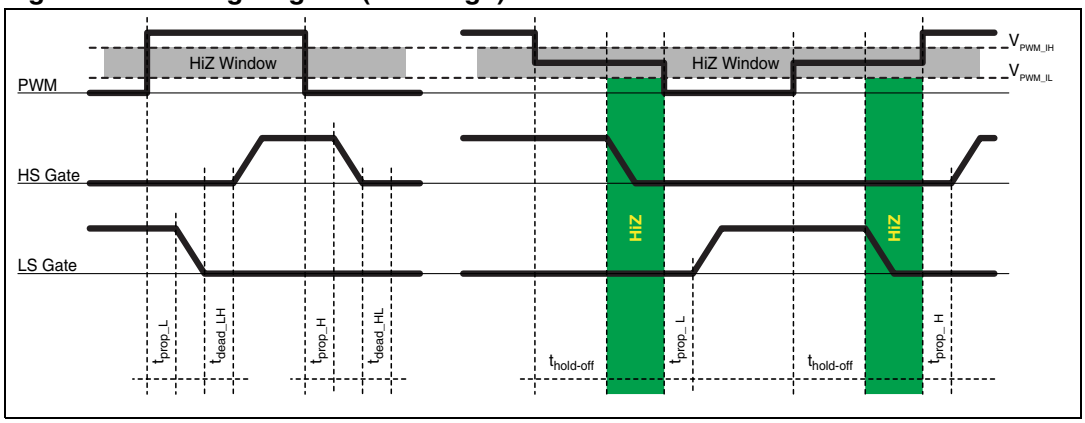
Before V_{CC} goes above the UVLO threshold, the L6747C keeps both the high-side and low-side MOSFETS firmly OFF. Then, after the UVLO has been crossed, the EN and PWM inputs take control over the driver's operations.

The EN pin enables the driver. If low, it keeps all MOSFETs OFF (HiZ) regardless of the status of PWM. When EN is high, the PWM input takes control. If externally set within the HiZ window, the driver enters an HiZ state and both MOSFETS are kept in an OFF state until PWM exits the HiZ window (see *Figure 4*).

After the UVLO threshold has been crossed and while in HiZ, the preliminary OV protection is activated. If the voltage sensed through the PHASE pin goes above about 1.8 V, the low-side MOSFET is latched ON in order to protect the load from dangerous overvoltage. The driver status is reset from a PWM transition.

Driver power supply, as well as power conversion input, are flexible: 5 V and 12 V can be chosen for high-side and low-side MOSFET voltage drive.

Figure 4. Timing diagram (EN = High)



4.1 High-impedance (HiZ) management

The driver is capable of managing a high-impedance conditions by keeping all MOSFETs in an OFF state. This is achieved in two different ways:

- If the EN signal is pulled low, the device keeps all MOSFETs OFF regardless of the PWM status.
- When EN is asserted, if the PWM signal is externally set within the HiZ window for a time greater than the hold-off time, the device detects the HiZ condition and turns off all the MOSFETs. The HiZ window is defined as the PWM voltage range between $V_{PWM\_HIZ\_H}$ = 1.6 V and $V_{PWM\_HIZ\_L}$ = 1.3 V.

The device exits from the HiZ state after any PWM transition. See *Figure 4* for details about HiZ timing.

The implementation of the high-impedance state allows the controller connected to the driver to manage the high-impedance state of its output, preventing the generation of negative undershoot on the regulated voltage during the shutdown stage. Also, different power management states may be managed, such as pre-bias startup.

4.2 Preliminary OV protection

When V_{CC} exceeds its UVLO threshold while the device is in HiZ, the L6747C activates the preliminary OV protection.

The intent of this protection feature is to protect the load during system startup, especially from high-side MOSFET failures. In fact, VRM, and more generally PWM, controllers, have a 12 V bus-compatible turn-on threshold and are non-operative if V_{CC} is below the turn-on thresholds (which is in the range of about 10 V). In cases of high-side MOSFET failure, the controller does not recognize the overvoltage until V_{CC} = ~10 V (unless other special features are implemented). However, in this case the output voltage is already at the same voltage (~10 V) and the load (a CPU in most cases) is already burnt.

The L6747C bypasses the PWM controller by latching on the low-side MOSFET if the PHASE pin voltage exceeds 2 V during the HiZ state. When the PWM input exits from the HiZ window, the protection is reset and the control of the output voltage is transferred to the controller connected to the PWM input.

Since the driver has its own UVLO threshold, a simple way to provide protection to the output in all conditions when the device is OFF is to supply the controller through the 5 V_{SB} bus. 5 V_{SB} is always present before any other voltage and, in case of high-side short, the low-side MOSFET is driven with 5 V. This ensures reliable protection of the load.

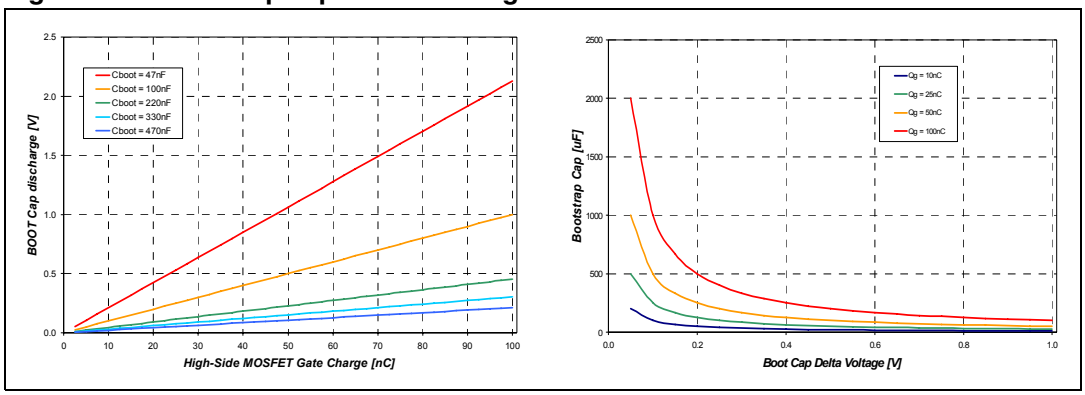
Preliminary OV is active after UVLO and while the driver is in an HiZ state, and it is disabled after the first PWM transition. The controller must manage its output voltage from that moment on.

4.3 BOOT capacitance design

The bootstrap capacitor value should be selected to obtain a negligible discharge due to the turning on of the high-side MOSFET. It must provide a stable voltage supply to the high-side driver during the MOSFET turn-on, and minimize the power dissipated by the embedded boot diode. *Figure 5* illustrates some guidelines on how to select the capacitance value for the bootstrap according to the desired discharge, and the selected MOSFET.

To prevent the bootstrap capacitor from overcharging as a consequence of large negative spikes, an external series R_{BOOT} resistor (in the range of few ohms) may be required in series with the BOOT pin.

Figure 5. Bootstrap capacitance design



4.4 Power dissipation

The L6747C embeds high current drivers for both high-side and low-side MOSFETs. It is therefore important to consider the power that the device is going to dissipate in driving them in order to avoid exceeding the maximum junction operating temperature.

Two main factors contribute to device power dissipation: bias power and driver power.

- Device power (P_{DC}) depends on the static consumption of the device through the supply pins and is easily quantifiable as follows:

$$P_{DC} = V_{CC} \cdot I_{CC} + V_{PVCC} \cdot I_{PVCC}$$

- Driver power is the power needed by the driver to continuously switch the external MOSFETs ON and OFF. It is a function of the switching frequency and total gate charge of the selected MOSFETs. It can be quantified considering that the total power P_{SW} dissipated to switch the MOSFETs is influenced by three main factors: external gate resistance (when present), intrinsic MOSFET resistance, and intrinsic driver resistance. This last factor is the important one to be determined to calculate the device power dissipation.

The total power dissipated to switch the MOSFETs is:

$$P_{SW} = F_{SW} \cdot (Q_{GHS} \cdot PVCC + Q_{GLS} \cdot VCC)$$

When designing an application based on the L6747C it is recommended to take into consideration the effect of external gate resistors on the power dissipated by the driver. External gate resistors help the device to dissipate the switching power since the same power P_{SW} is shared between the internal driver impedance and the external resistor, resulting in a general cooling of the device.

Referring to *Figure 6*, a classic MOSFET driver can be represented by a push-pull output stage with two different MOSFETs: a P-MOSFET to drive the external gate high, and an N-MOSFET to drive the external gate low (with their own $R_{DS(on)}$: R_{hi_HS}, R_{lo_HS}, R_{hi_LS}, R_{lo_LS}). The external power MOSFET can be represented in this case as a capacitance (C_{G_HS}, C_{G_LS}) that stores the gate-charge (Q_{G_HS}, Q_{G_LS}) required by the external power

MOSFET to reach the driving voltage (PVCC for HS and VCC for LS). This capacitor is charged and discharged at the driver switching frequency F_{SW}.

The total power P_{SW} is dissipated among the resistive components distributed along the driving path. According to the external gate resistance and the power MOSFET intrinsic gate resistance, the driver dissipates only a portion of P_{SW} as follows:

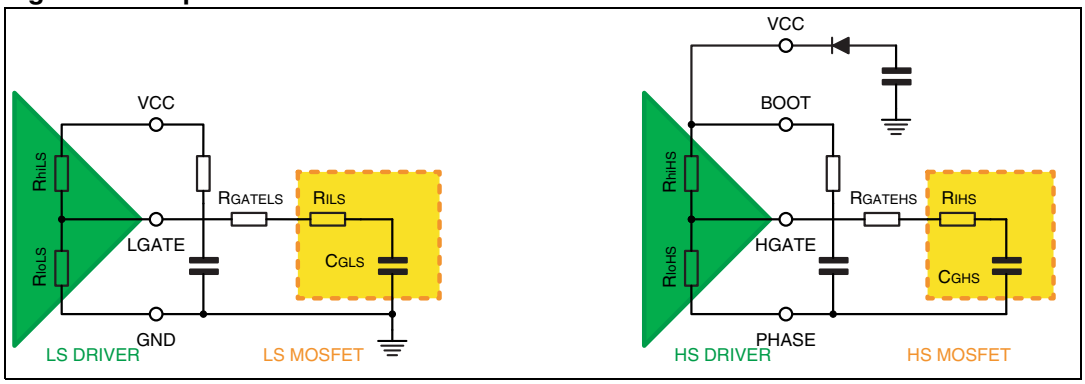
$$P_{SW-HS} = \frac{1}{2} \cdot C_{GHS} \cdot PVCC^2 \cdot Fsw \cdot \left(\frac{R_{hiHS}}{R_{hiHS} + R_{GateHS} + R_{iHS}} + \frac{R_{loHS}}{R_{loHS} + R_{GateHS} + R_{iHS}} \right)$$

$$P_{SW-LS} = \frac{1}{2} \cdot C_{GLS} \cdot VCC^2 \cdot Fsw \cdot \left(\frac{R_{hiLS}}{R_{hiLS} + R_{GateLS} + R_{iLS}} + \frac{R_{loLS}}{R_{loLS} + R_{GateLS} + R_{iLS}} \right)$$

The total power dissipated from the driver can then be determined as follows:

$$P = P_{DC} + P_{SW-HS} + P_{SW-LS}$$

Figure 6. Equivalent circuit for a MOSFET driver



4.5 Layout guidelines

L6747C provides driving capability to implement high-current step-down DC-DC converters.

The first priority when placing components for these applications should be given to the power section, minimizing the length of each connection and loop as much as possible. To minimize noise and voltage spikes (as well as EMI and losses) power connections must be part of a power plane, and in any case constructed with wide and thick copper traces. The loop must be minimized. The critical components, such as the power MOSFETs, must be close to each other. However, some space between the power MOSFETs is required to assure good thermal cooling and airflow.

Traces between the driver and the MOSFETS should be short and wide to minimize the inductance of the trace, which in turn minimizes ringing in the driving signals. Moreover, the VIA count should be minimized to reduce the related parasitic effect.

The use of a multi-layer printed circuit board is recommended.

Small signal components and connections to critical nodes of the application, as well as bypass capacitors for the device supply, are also important. Place the bypass capacitor

(VCC, PVCC and BOOT capacitors) close to the device with the shortest possible loop, using wide copper traces to minimize parasitic inductance.

Systems that do not use Schottky diodes in parallel with the low-side MOSFET might show large negative spikes on the PHASE pin. This spike can be limited, as can the positive spike, but has an additional consequence: it causes the bootstrap capacitor to be overcharged. This extra charge can cause, in the worst case condition of maximum input voltage and during particular transients, that boot-to-phase voltage exceeds the absolute maximum ratings causing device failures. It is therefore suggested in this cases to limit this extra charge by adding a small R_{BOOT} resistor in series with the boot capacitor. The use of R_{BOOT} also contributes in the limitation of the spike present on the BOOT pin.

For heat dissipation, place the copper area under the IC. This copper area may be connected by internal copper layers through several VIAs to improve thermal conductivity. The combination of copper pad, copper plane and VIAs under the driver allows the device to achieve its best thermal performance.

Figure 7. Driver turn-on and turn-off paths

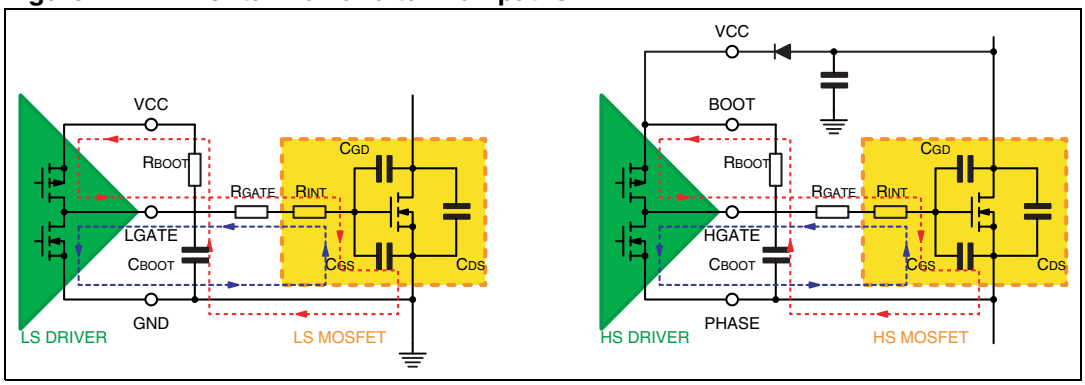
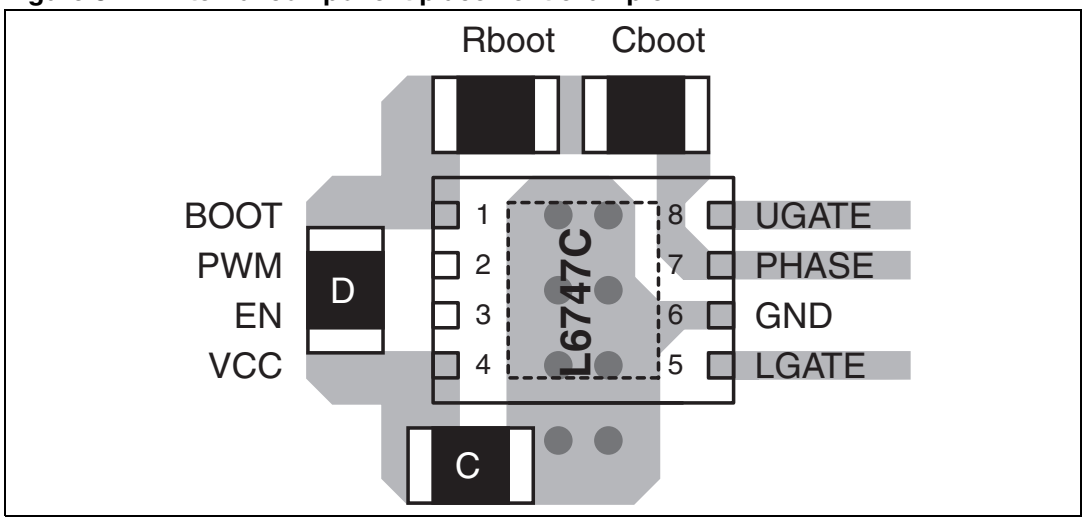


Figure 8. External component placement example



5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

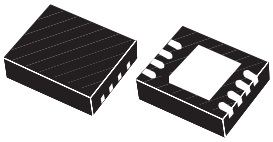
Figure 9. VFDFPN8 mechanical data and package dimensions

DIMENSIONS						
REF.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.80	0.90	1.00	31.49	35.43	39.37
A1		0.02	0.05		0.787	1.968
A2	0.55	0.65	0.80	21.65	25.59	31.49
A3		0.20			7.874	
b	0.18	0.25	0.30	7.086	9.842	11.81
D	2.85	3.00	3.15	112.2	118.1	124.0
D2	2.20		2.70	86.61		106.3
E	2.85	3.00	3.15	112.2	118.1	124.0
E2	1.40		1.75	55.11		68.89
e		0.50			19.68	
L	0.30	0.40	0.50	11.81	15.74	19.68
ddd			0.08			3.149

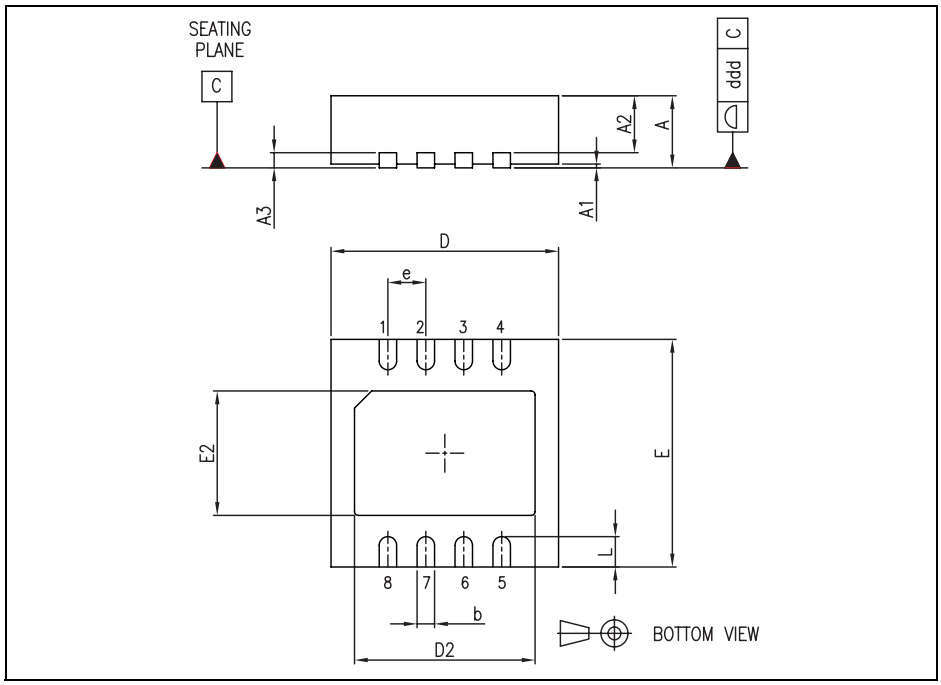
PACKAGE AND PACKING INFORMATION

Very thin Fine pitch Dual Flat Package no Lead

Weight: not available



VFDFPN8 (3x3)



6 Revision history

Table 6. Document revision history

Date	Revision	Changes
23-Apr-2010	1	Initial release.

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