

DALLAS
SEMICONDUCTORT-46-23-37
DS1230Y/AB

256K Nonvolatile SRAM

FEATURES

- Data retention in the absence of V_{CC}
- Data is automatically protected during the decrease in V_{CC} at power loss
- Directly replaces 32K x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- Over 10 years of data retention
- Standard 28-pin JEDEC pinout
- Available in 70ns, 100ns, 120ns, 150ns, or 200ns read access times
- Read cycle time equals write cycle time
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional $\pm 5\%$ and $\pm 10\%$ operating range

PIN DESCRIPTION

A14	1	28	V_{CC}
A12	2	27	WE\
A7	3	26	A13
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	OE\
A2	8	21	A10
A1	9	20	CE\
A0	10	19	DQ7
DQ0	11	18	DQ6
DQ1	12	17	DQ5
DQ2	13	16	DQ4
GND	14	15	DQ3

28-Pin Encapsulated Package
(720 Mil Extended)**PIN NAMES (\ Denotes Condition Low)**

A0 - A14	- Address Inputs
CE\	- Chip Enable
GND	- Ground
DQ0-DQ7	- Data In/Data Out
V_{CC}	- Power (+5V)
WE\	- Write Enable
OE\	- Output Enable

DESCRIPTION

The DS1230AB and DS1230Y 256K Non-volatile SRAMs are 262,144-bit, fully static, nonvolatile RAMs organized as 32,768 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry that constantly monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protec-

tion is unconditionally enabled to prevent garbled data. The NV SRAM can be used in place of existing 32K x 8 static RAMs directly conforming to the popular byte-wide 28-pin DIP standard. The DS1230AB also matches the pinout of the 28256 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interface.

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READ MODE

The DS1230AB and DS1230Y execute a read cycle whenever WE\ (Write Enable) is inactive (high) and CE\ (Chip Enable) is active (low). The unique address specified by the 15 address inputs (A_0 - A_{14}) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within t_{ACC} (Access Time) after the last address input signal is stable, providing that CE\ and OE\ (Output Enable) access times are also satisfied. If OE\ and CE\ access times are not satisfied, then data access must be measured from the later occurring signal (CE\ or OE\) and the limiting parameter is either t_{CO} for CE\ or t_{OE} for OE\ rather than address access.

WRITE MODE

The DS1230AB and DS1230Y are in the write mode whenever the WE\ and CE\ signals are in the active (low) state after address inputs are stable. The latter occurring falling edge of CE\ or WE\ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of CE\ or WE\ . All address inputs must be kept valid throughout the write cycle. WE\ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The OE\ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled (CE\ and OE\ active) then WE\ will disable the outputs in t_{ODW} from its falling edge.

DATA RETENTION MODE

The DS1230AB provides full functional capability for V_{CC} greater than 4.75 volts and write protects at 4.5 volts. The DS1230Y provides full functional capability for V_{CC} greater than 4.5 volts and write protects by 4.25 volts. Data is

maintained in the absence of V_{CC} without any additional support circuitry. The nonvolatile static RAM constantly monitors V_{CC} . Should the supply voltage decay, the RAM automatically write protects itself. All inputs to the RAM become "don't care" and all outputs are high impedance. As V_{CC} falls below approximately 3.0 volts, the power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0 volts, the power switching circuit connects external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5 volts for DS1230Y and 4.75 volts for the DS1230AB.

FRESHNESS SEAL AND BATTERY REDUNDANCY

The DS1230Y and DS1230AB are shipped from Dallas Semiconductor with the lithium energy source disconnected, guaranteeing full energy capacity. When V_{CC} is first applied at a level of greater than 4.25 volts, the lithium energy source is enabled for battery back-up operation.

Battery redundancy is also provided to ensure reliability. The DS1230Y and DS1230AB contain two lithium energy cells separated by an internal isolation switch. During battery backup time the cell with the highest voltage is selected for use. If one battery fails, the other battery automatically takes over. The switch between batteries is transparent to the user.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to +70°C
Soldering Temperature	260°C for 10 sec.

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
DS1230AB Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
DS1230Y Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input Logic 1	V_{IH}	2.2		V_{CC}	V	
Input Logic 0	V_{IL}	0.0		0.8	V	

DC ELECTRICAL CHARACTERISTICS(0°C to 70°C; $V_{CC} = 5V \pm 10\%$ for DS1230Y)(0°C to 70°C; $V_{CC} = 5V \pm 5\%$ for DS1230AB)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	I_{IL}	-1.0		+1.0	μA	
I/O Leakage Current $CE \geq V_{IH} \leq V_{CC}$	I_{IO}	-1.0		+1.0	μA	
Output Current @ 2.4V	I_{OH}	-1.0			mA	
Output Current @ 0.4V	I_{OL}	2.0			mA	
Standby Current $CE \leq 2.2V$	I_{CCS1}		5.0	10	mA	
Standby Current $CE \leq V_{CC} - 0.5V$	I_{CCS2}		3.0	5.0	mA	
Operating Current $t_{CYC} = 200ns$	I_{CCO1}			85	mA	
Write Protection Voltage (DS1230AB)	V_{TP}	4.5	4.62	4.75	V	
Write Protection Voltage (DS1230Y)	V_{TP}	4.25	4.37	4.5	V	

DC Test Conditions:

Outputs open; all voltages are referenced to ground.

CAPACITANCE(t_A = 25°C)

PARAMETER	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	10	pF	
Input/Output Capacitance	C_{IO}	5	10	pF	

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AC ELECTRICAL CHARACTERISTICS (0°C to 70°C; $V_{CC}=5.0V \pm 10\%$ for DS1230Y)
 (0°C to 70°C; $V_{CC}=5.0V \pm 5\%$ for DS1230AB)

PARAMETER	SYM	DS1230Y-70 1230AB-70		DS1230Y-100 1230AB-100		DS1230Y-120 1230AB-120		DS1230Y-150 1230AB-150		DS1230Y-200 DS1230AB-200		U	N
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	t_{RO}	70		100		120		150		200		ns	
Access Time	t_{ACC}		70		100		120		150		200	ns	
OE\ to Output Valid	t_{OE}		35		50		60		70		100	ns	
CE\ to Output Valid	t_{CO}		70		100		120		150		200	ns	
OE\ or CE\ to Output Active	t_{COE}	5		5		5		5		5		ns	5
Output High Z from Deselection	t_{OD}		25		35		40		70		100	ns	5
Output Hold from Address Change	t_{OH}	5		5		5		5		5		ns	
Write Cycle Time	t_{WC}	70		100		120		150ns		200		ns	
Write Pulse Width	t_{WP}	55		75		90		100		100		ns	3
Address Setup Time	t_{AW}	0		0		0		0		0		ns	
Write Recovery Time	t_{WR}	20		20		20		20		20		ns	
Output High Z from WE\	t_{ODW}		25		35		40		70		80	ns	5
Output Active from WE\	t_{OEW}	5		5		5		5		5		ns	5
Data Setup Time	t_{DS}	30		40		50		60		80		ns	4
Data Hold Time from WE\	t_{DH}	20		20		20		20		20		ns	4

AC Test Conditions

Output Load: 100 pF + 1TTL Gate

Input Pulse Levels: 0-3.0V

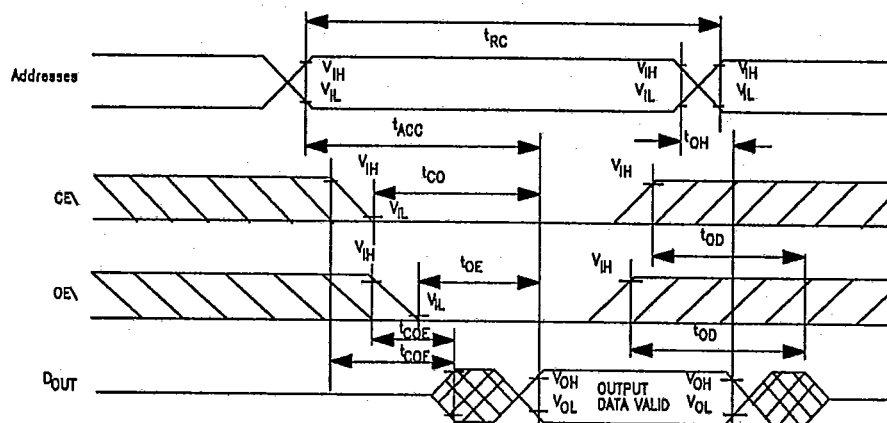
Timing Measurement Reference Levels

Input: 1.5V Output: 1.5V

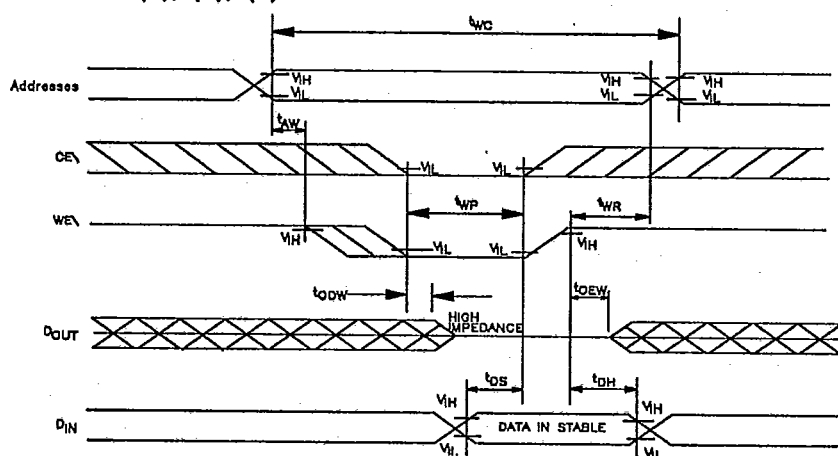
Input Pulse Rise and Fall Times: 5ns

READ CYCLE (1)

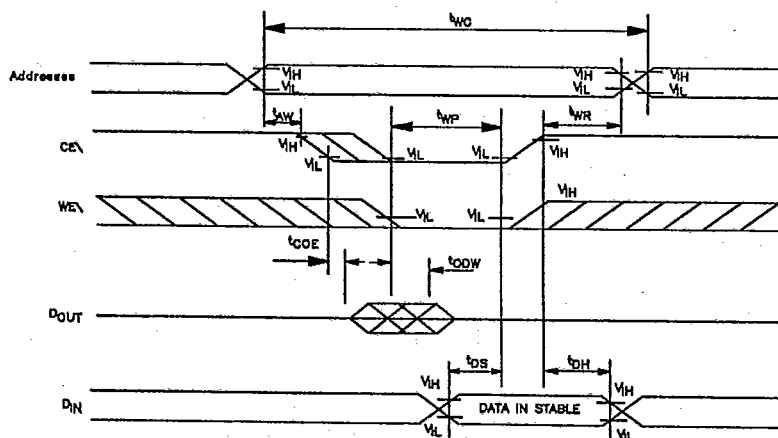
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WRITE CYCLE 1 (2), (6), (7)

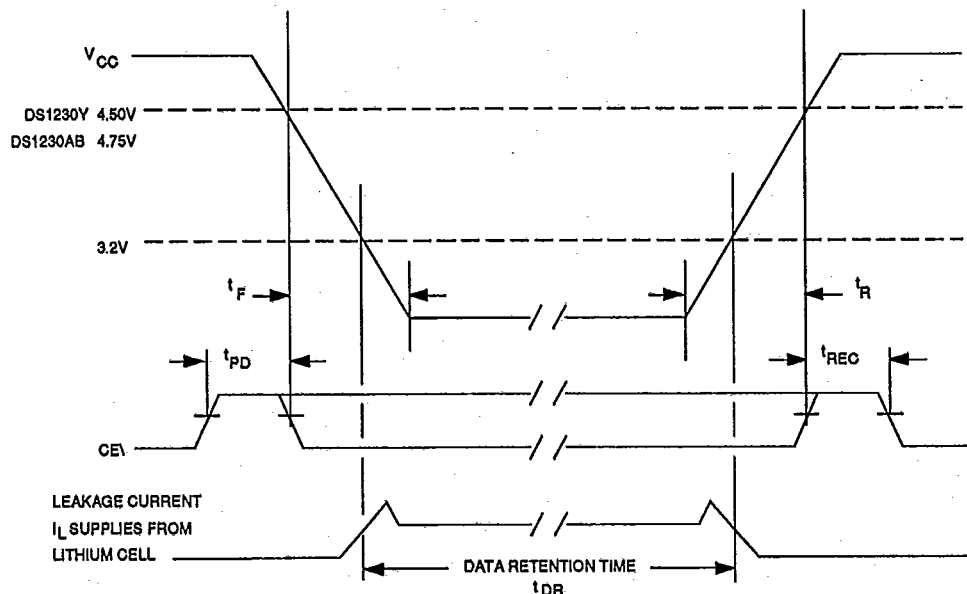


WRITE CYCLE 2 (2), (8)



POWER-DOWN/POWER-UP CONDITION

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POWER-DOWN/POWER-UP TIMING

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{PD}	CE\ at V_{IH} before Power-Down	0		μs	
t_F	V_{CC} Slew from 4.75V to 0V (CE\ at V_{IH})	300		μs	DS1230AB
t_F	V_{CC} Slew from 4.5V to 0V (CE\ at V_{IH})	300		μs	DS1230Y
t_R	V_{CC} Slew from 0V to 4.75V (CE\ at V_{IH})	0		μs	DS1230AB
t_R	V_{CC} Slew from 0V to 4.5V (CE\ at V_{IH})	0		μs	DS1230Y
t_{REC}	CE\ at V_{IH} after Power-Up	2	125	ms	

($t_A=25^\circ C$)

SYM	PARAMETER	MIN	MAX	UNITS	NOTES
t_{DR}	Expected Data Retention Time	10		years	9

WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

NOTES

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1. $WE\backslash$ is high for a read cycle.
2. $OE\backslash = V_{IH}$ or V_{IL} . If $OE\backslash = V_{IH}$ during write cycle, the output buffers remain in a high impedance state.
3. t_{WP} is specified as the logical AND of $CE\backslash$ and $WE\backslash$.
 t_{WP} is measured from the latter of $CE\backslash$ or $WE\backslash$ going low to the earlier of $CE\backslash$ or $WE\backslash$ going high.
4. t_{DH} , t_{DS} are measured from the earlier of $CE\backslash$ or $WE\backslash$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $CE\backslash$ low transition occurs simultaneously with or later than the $WE\backslash$ low transition in Write Cycle 1, the output buffers remain in a high impedance state during this period.
7. If the $CE\backslash$ high transition occurs prior to or simultaneously with the $WE\backslash$ high transition, the output buffers remain in a high impedance state during this period.
8. If $WE\backslash$ is low or the $WE\backslash$ low transition occurs prior to or simultaneously with the $CE\backslash$ low transition, the output buffers remain in a high impedance state during this period.
9. Each DS1230 has a built-in switch that disconnects the lithium source until V_{CC} is first applied by the user. The expected t_{DR} is defined as accumulative time in the absence of V_{CC} starting from the time power is first applied by the user.