LM101A/LM201A/LM301A Operational Amplifiers

Check for Samples: LM101A-N, LM201A-N, LM301A-N

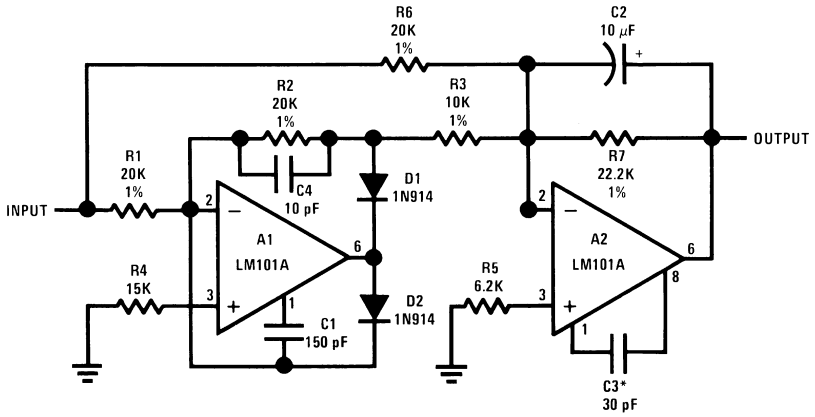
FEATURES

- **Offset voltage 3 mV maximum over temperature (LM101A/LM201A)**
- **Input current 100 nA maximum over temperature (LM101A/LM201A)**
- **Offset current 20 nA maximum over temperature (LM101A/LM201A)**
- **Guaranteed drift characteristics**
- **Offsets guaranteed over entire common mode and supply voltage ranges**
- **Slew rate of 10V/μs as a summing amplifier**
  - **This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, and freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the frequency compensation can be tailored to the particular application. For example, in low frequency circuits it can be overcompensated for increased stability margin. Or the compensation can be optimized to give more than a factor of ten improvement in high frequency performance for most applications.**
  - **In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and a drift at a lower cost.**
  - **The LM101A is ensured over a temperature range of −55°C to +125°C, the LM201A from −25°C to +85°C, and the LM301A from 0°C to +70°C.**

DESCRIPTION

The LM101A series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. Advanced processing techniques make possible an order of magnitude reduction in input currents, and a redesign of the biasing circuitry reduces the temperature drift of input current. Improved specifications include:

Fast AC/DC Converter



Feedforward compensation can be used to make a fast full wave rectifier without a filter.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

	LM101A/LM201A	LM301A
Supply Voltage	±22V	±18V
Differential Input Voltage	±30V	±30V
Input Voltage (2)	±15V	±15V
Output Short Circuit Duration (3)	Continuous	Continuous
Operating Ambient Temp. Range	−55°C to +125°C (LM101A)	0°C to +70°C
	−25°C to +85°C (LM201A)	
T_J Max		
H-Package	150°C	100°C
N-Package	150°C	100°C
J-Package	150°C	100°C
Power Dissipation at T_A = 25°C		
H-Package (Still Air)	500 mW	300 mW
(400 LF/Min Air Flow)	1200 mW	700 mW
N-Package	900 mW	500 mW
J-Package	1000 mW	650 mW
Thermal Resistance (Typical) θ_{jA}		
H-Package (Still Air)	165°C/W	165°C/W
(400 LF/Min Air Flow)	67°C/W	67°C/W
N Package	135°C/W	135°C/W
J-Package	110°C/W	110°CmW
(Typical) θ_{jC}		
H-Package	25°C/W	25°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)		
Metal Can or Ceramic	300°C	300°C
Plastic	260°C	260°C
ESD Tolerance (4)	2000V	2000V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.Operating ratings indicate for which the device is functional, but do no guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

(2) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

(3) Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 75°C for LM101A/LM201A, and 70°C and 55°C respectively for LM301A.

(4) Human body model, 100 pF discharged through 1.5 kΩ.

Electrical Characteristics (1)

$T_A = T_J$

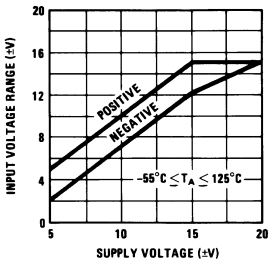
Parameter	Conditions		LM101A/LM201A			LM301A			Units
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C, R_S ≤ 50 kΩ			0.7	2.0		2.0	7.5	mV
Input Offset Current	T_A = 25°C			1.5	10		3.0	50	nA
Input Bias Current	T_A = 25°C			30	75		70	250	nA
Input Resistance	T_A = 25°C		1.5	4.0		0.5	2.0		MΩ
Supply Current	T_A = 25°C	V_S = ±20V		1.8	3.0				mA
		V_S = ±15V					1.8	3.0	mA
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15V		50	160		25	160		V/mV
	V_{OUT} = ±10V, R_L ≥ 2 kΩ								
Input Offset Voltage	R_S ≤ 50 kΩ				3.0			10	mV
Average Temperature Coefficient	R_S ≤ 50 kΩ			3.0	15		6.0	30	µV/°C
of Input Offset Voltage									
Input Offset Current					20			70	nA
Average Temperature Coefficient	25°C ≤ T_A ≤ T_{MAX}			0.01	0.1		0.01	0.3	nA/°C
of Input Offset Current	T_{MIN} ≤ T_A ≤ 25°C			0.02	0.2		0.02	0.6	nA/°C
Input Bias Current					0.1			0.3	µA
Supply Current	T_A = T_{MAX}, V_S = ±20V			1.2	2.5				mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V		25			15			V/mV
	R_L ≥ 2k								
Output Voltage Swing	V_S = ±15V	R_L = 10 kΩ	±12	±14		±12	±14		V
		R_L = 2 kΩ	±10	±13		±10	±13		V
Input Voltage Range	V_S = ±20V		±15						V
	V_S = ±15V			+15, −13		±12	+15, −13		V
Common-Mode Rejection Ratio	R_S ≤ 50 kΩ		80	96		70	90		dB
Supply Voltage Rejection Ratio	R_S ≤ 50 kΩ		80	96		70	96		dB

(1) Unless otherwise specified, these specifications apply for C1 = 30 pF, ±5V ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ +125°C (LM101A), ±5V ≤ V_S ≤ ±20V and −25°C ≤ T_A ≤ +85°C (LM201A), ±5V ≤ V_S ≤ ±15V and 0°C ≤ T_A ≤ +70°C (LM301A).

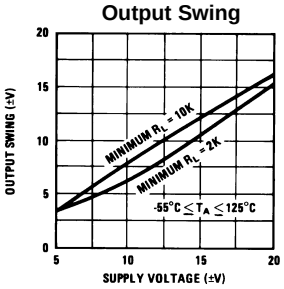
Typical Performance Characteristics

LM101A/LM201A

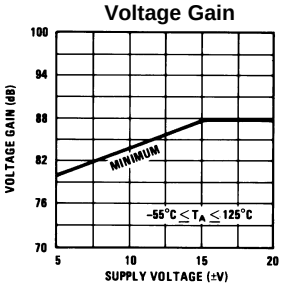
Input Voltage Range



Output Swing



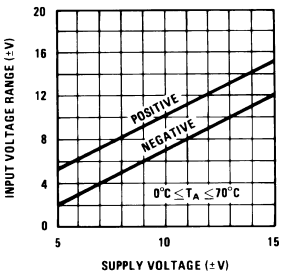
Voltage Gain



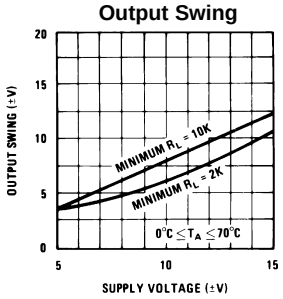
Guaranteed Performance Characteristics

LM301A

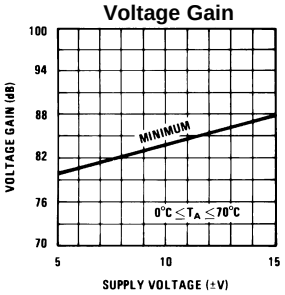
Input Voltage Range



Output Swing

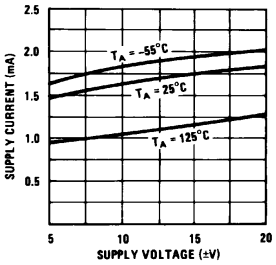


Voltage Gain

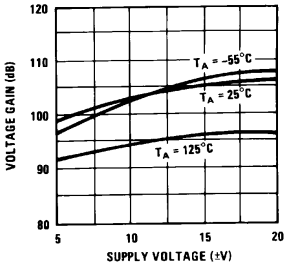


Typical Performance Characteristics

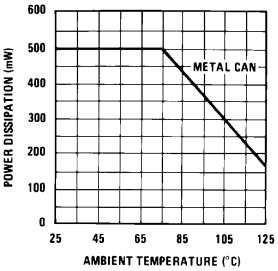
Supply Current



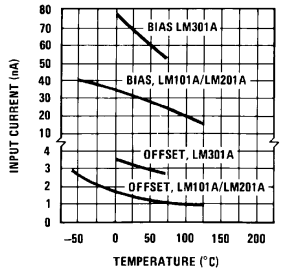
Voltage Gain



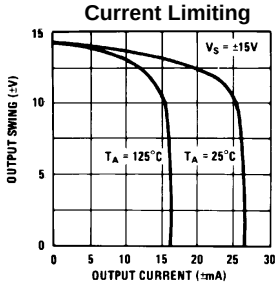
Maximum Power Dissipation



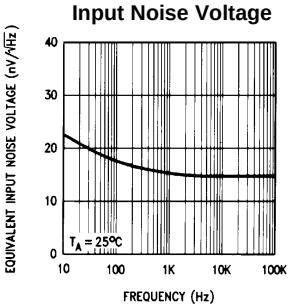
Input Current, LM101A/LM201A/LM301A



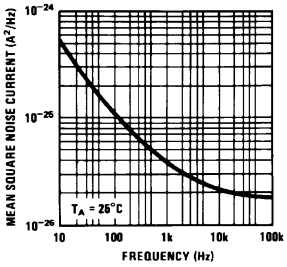
Current Limiting



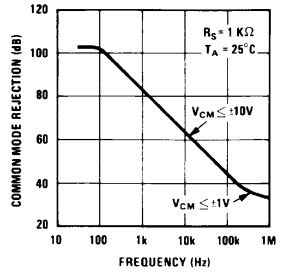
Input Noise Voltage



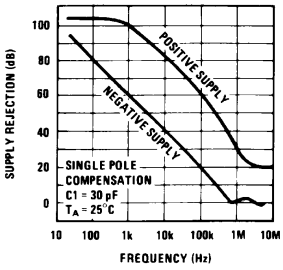
Input Noise Current



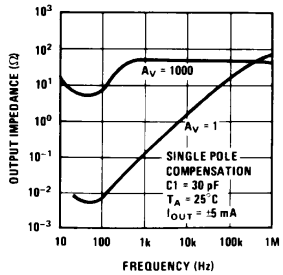
Common Mode Rejection



Power Supply Rejection

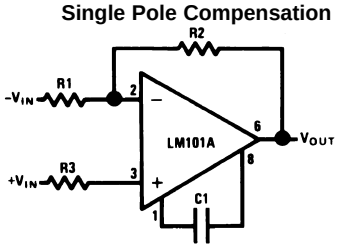


Closed Loop Output Impedance



Typical Performance Characteristics for Various Compensation Circuits

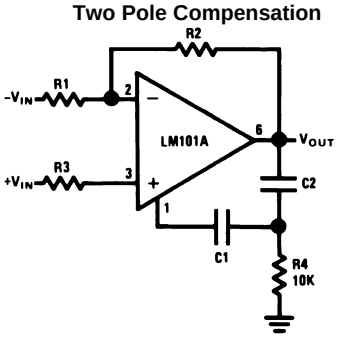
Single Pole Compensation



$$C1 \geq \frac{R1\,C_S}{R1 + R2}$$

C_S= 30 pF

Two Pole Compensation

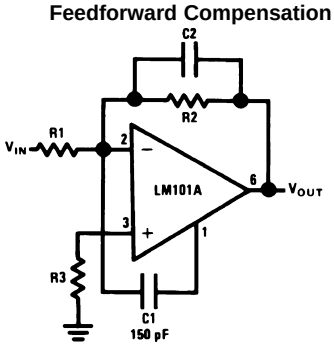


$$C1 \geq \frac{R1\,C_S}{R1 + R2}$$

C_S= 30 pF

C2 = 10 C1

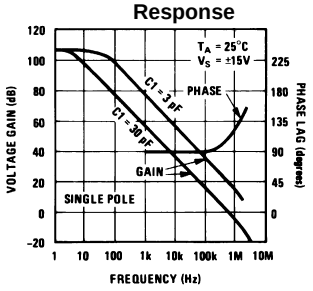
Feedforward Compensation



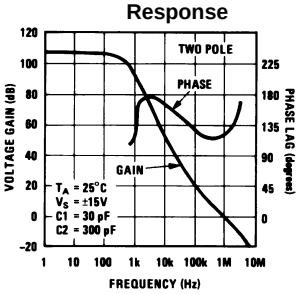
$$C2 = \frac{1}{2\pi\, f_o\, R2}$$

f_o= 3 MHz

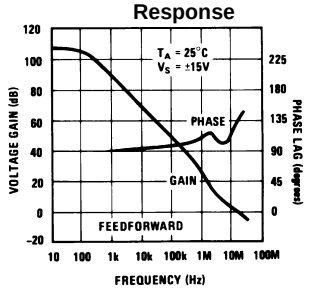
Open Loop Frequency Response



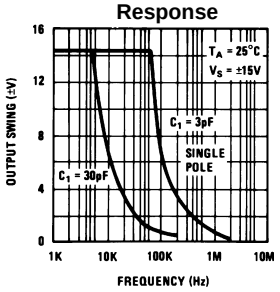
Open Loop Frequency Response



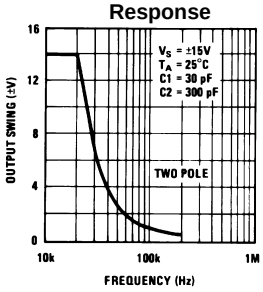
Open Loop Frequency Response



Large Signal Frequency Response

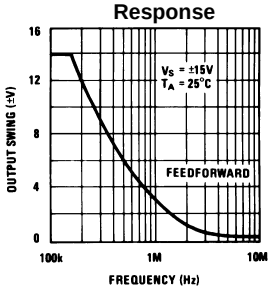


Large Signal Frequency Response

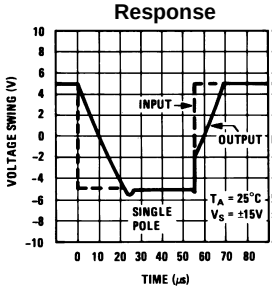


Typical Performance Characteristics for Various Compensation Circuits (continued)

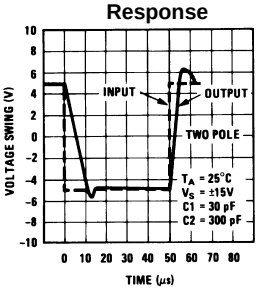
Large Signal Frequency Response



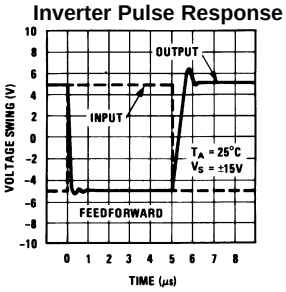
Voltage Follower Pulse Response



Voltage Follower Pulse Response

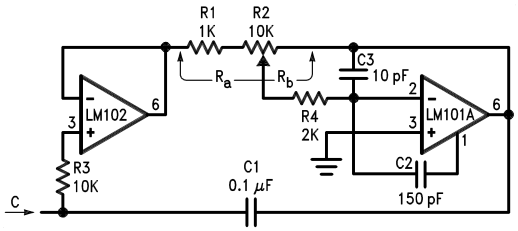


Inverter Pulse Response



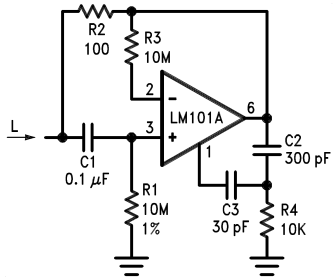
Typical Applications

Figure 1. Variable Capacitance Multiplier



$$C = 1 + \frac{R_b}{R_a} C1$$

Figure 2. Simulated Inductor



$L \simeq R1\ R2\ C1$

$R_S = R2$

$R_P = R1$

Figure 3. Fast Inverting Amplifier with High Input Impedance

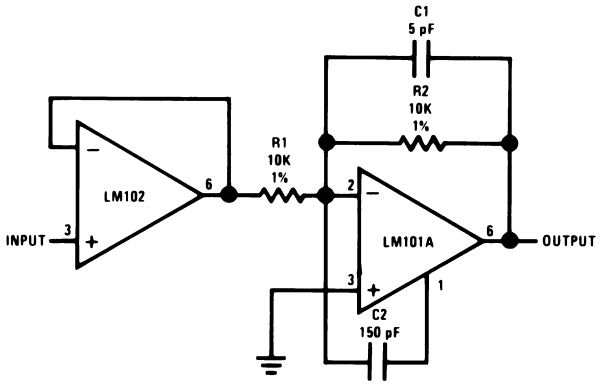
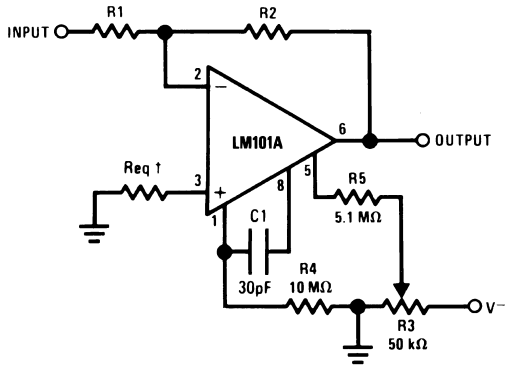
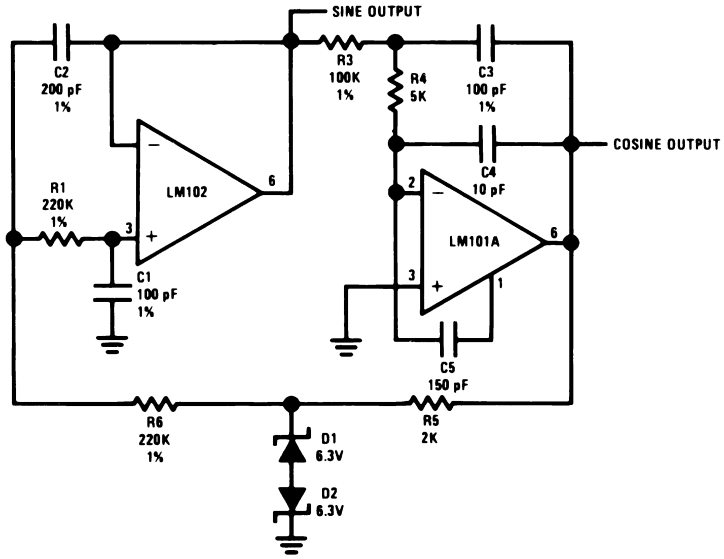


Figure 4. Inverting Amplifier with Balancing Circuit



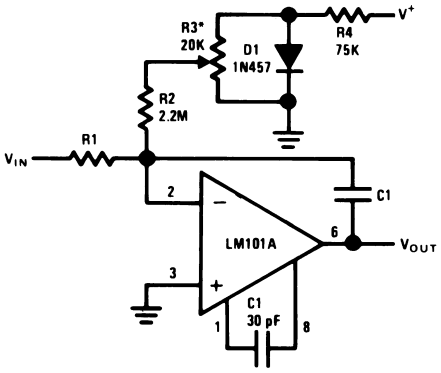
†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

Figure 5. Sine Wave Oscillator



f_o = 10 kHz

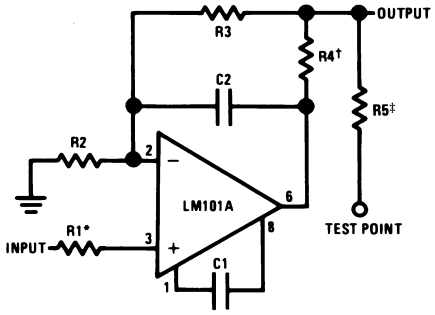
Figure 6. Integrator with Bias Current Compensation



*Adjust for zero integrator drift. Current drift typically 0.1 nA/°C over −55°C to +125°C temperature range.

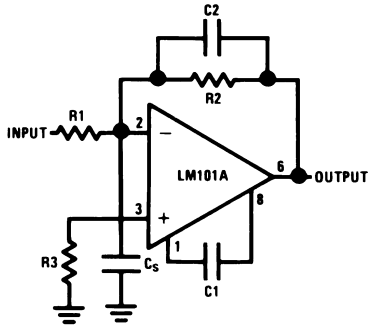
Application Hints

Figure 7. Protecting Against Gross Fault Conditions



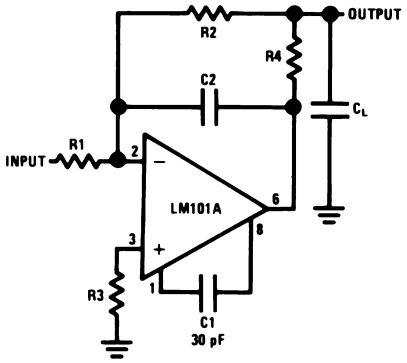
*Protects input
†Protects output
‡Protects output—not needed when R4 is used.

Figure 8. Compensating for Stray Input Capacitances or Large Feedback Resistor



$$C2 = \frac{R1\,C_S}{R2}$$

Figure 9. Isolating Large Capacitive Loads



Although the LM101A is designed for trouble free operation, experience has indicated that it is wise to observe certain precautions given below to protect the devices from abnormal operating conditions. It might be pointed out that the advice given here is applicable to practically any IC op amp, although the exact reason why may differ with different devices.

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak instantaneous output current of the source to something less than 100 mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Large capacitors on the input (greater than 0.1 µF) should be treated as a low source impedance and isolated with a resistor. Low impedance sources do not cause a problem unless their output voltage exceeds the supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

The output circuitry is protected against damage from shorts to ground. However, when the amplifier output is connected to a test point, it should be isolated by a limiting resistor, as test points frequently get shorted to bad places. Further, when the amplifer drives a load external to the equipment, it is also advisable to use some sort of limiting resistance to preclude mishaps.

Precautions should be taken to insure that the power supplies for the integrated circuit never become reversed—even under transient conditions. With reverse voltages greater than 1V, the IC will conduct excessive current, fusing internal aluminum interconnects. If there is a possibility of this happening, clamp diodes with a high peak current rating should be installed on the supply lines. Reversal of the voltage between V^+ and V^- will always cause a problem, although reversals with respect to ground may also give difficulties in many circuits.

The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF and capacitive loads smaller than 100 pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads.

Although the LM101A is relatively unaffected by supply bypassing, this cannot be ignored altogether. Generally it is necessary to bypass the supplies to ground at least once on every circuit card, and more bypass points may be required if more than five amplifiers are used. When feed-forward compensation is employed, however, it is advisable to bypass the supply leads of each amplifier with low inductance capacitors because of the higher frequencies involved.

TYPICAL APPLICATIONS

Figure 10. Standard Compensation and Offset Balancing Circuit

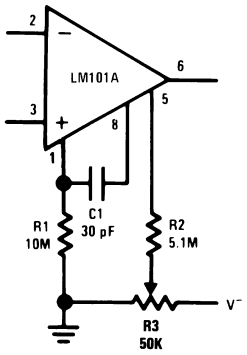
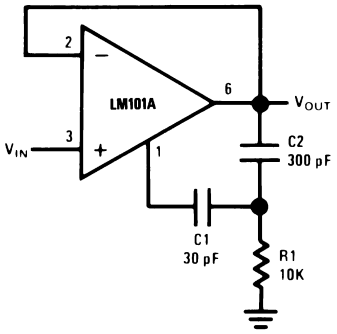
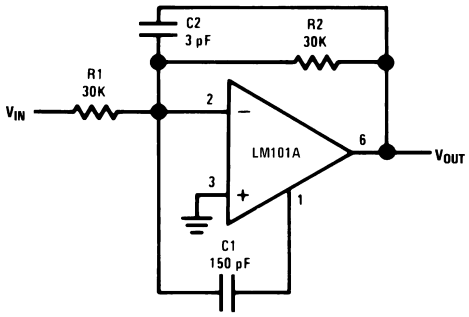


Figure 11. Fast Voltage Follower



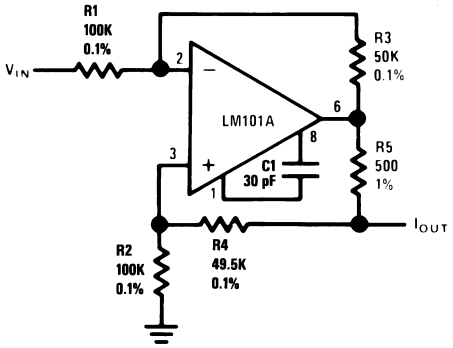
Power Bandwidth: 15 kHz
Slew Rate: 1V/μs

Figure 12. Fast Summing Amplifier



Power Bandwidth: 250 kHz
Small Signal Bandwiidth: 3.5 MHz
Slew Rate: 10V/μs

Figure 13. Bilateral Current Source

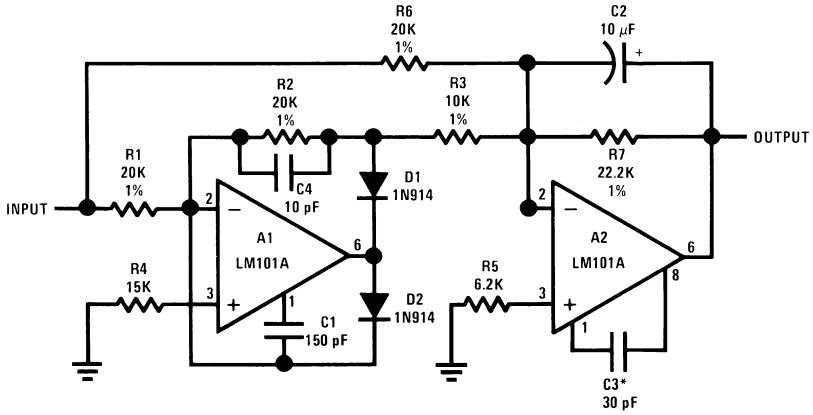


$$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$$

R3 = R4 + R5

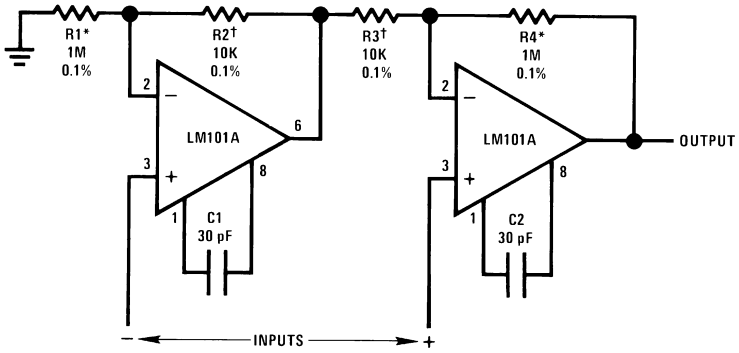
R1 = R2

Figure 14. Fast AC/DC Converter



Feedforward compensation can be used to make a fast full wave rectifier without a filter.

Figure 15. Instrumentation Amplifier

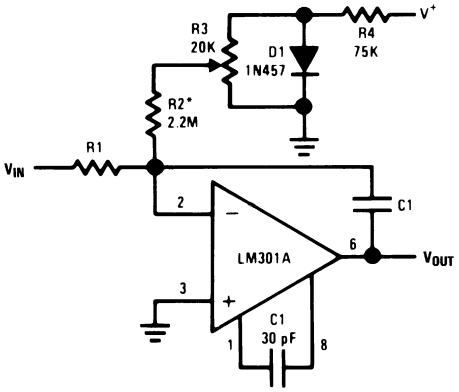


R1 = R4; R2 = R3

$$A_V = 1 + \frac{R1}{R2}$$

*,† Matching determines CMRR.

Figure 16. Integrator with Bias Current Compensation



*Adjust for zero integrator drift. Current drift typically 0.1 nA/°C over 0°C to +70°C temperature range.

Figure 17. Voltage Comparator for Driving RTL Logic or High Current Driver

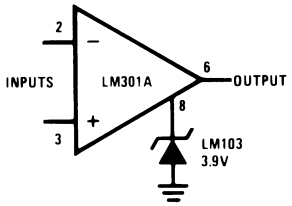


Figure 18. Low Frequency Square Wave Generator

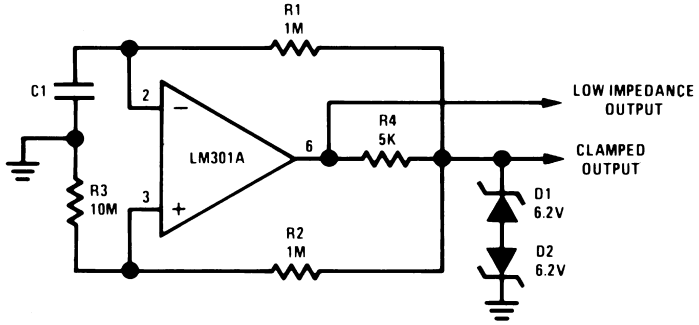
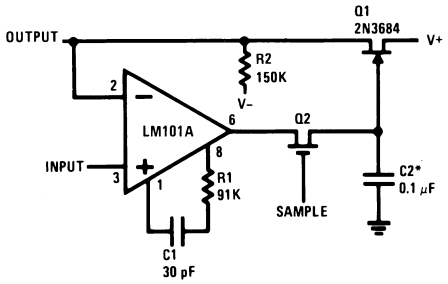
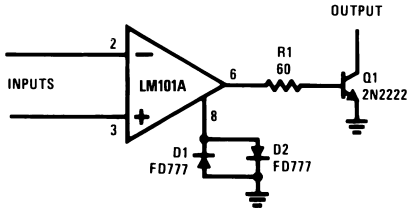


Figure 19. Low Drift Sample and Hold

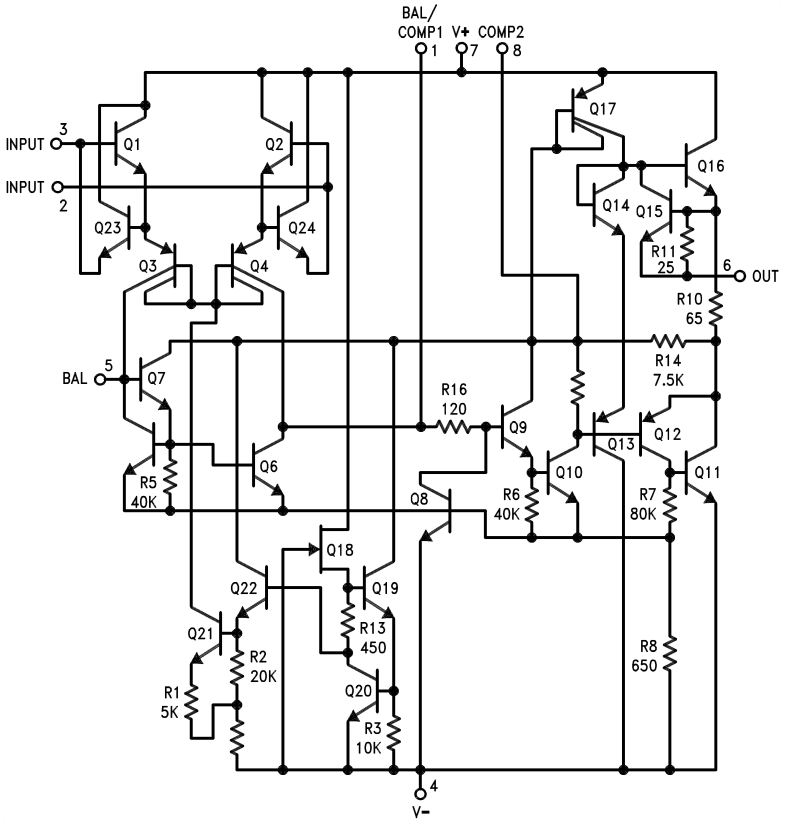


*Polycarbonate-dielectric capacitor

Figure 20. Voltage Comparator for Driving DTL or TTL Integrated Circuits



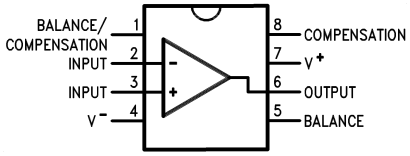
Schematic



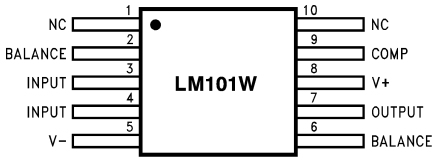
Pin connections shown are for 8-pin packages.

PIN DIAGRAMS

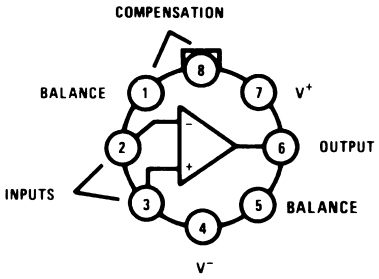
Dual-In-Line Package
(Top View)



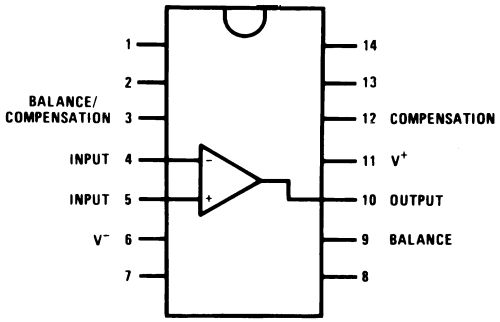
Ceramic Flatpack Package
(Top View)



Metal Can Package
(Top View)



Dual-In-Line Package
(Top View)



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
LM101AH	ACTIVE	TO-99	LMC	8	500	TBD	POST-PLATE	Level-1-NA-UNLIM	
LM101AH/NOPB	ACTIVE	TO-99	LMC	8	500	Green (RoHS & no Sb/Br)	POST-PLATE	Level-1-NA-UNLIM	
LM101AJ	ACTIVE	CDIP	NAB	8	40	TBD	Call TI	Level-1-NA-UNLIM	
LM201AH	ACTIVE	TO-99	LMC	8	500	TBD	POST-PLATE	Level-1-NA-UNLIM	
LM201AH/NOPB	ACTIVE	TO-99	LMC	8	500	Green (RoHS & no Sb/Br)	POST-PLATE	Level-1-NA-UNLIM	
LM301AH	ACTIVE	TO-99	LMC	8	500	TBD	POST-PLATE	Level-1-NA-UNLIM	
LM301AH/NOPB	ACTIVE	TO-99	LMC	8	500	Green (RoHS & no Sb/Br)	POST-PLATE	Level-1-NA-UNLIM	
LM301AN	ACTIVE	PDIP	P	8	40	TBD	Call TI	Level-1-NA-UNLIM	
LM301AN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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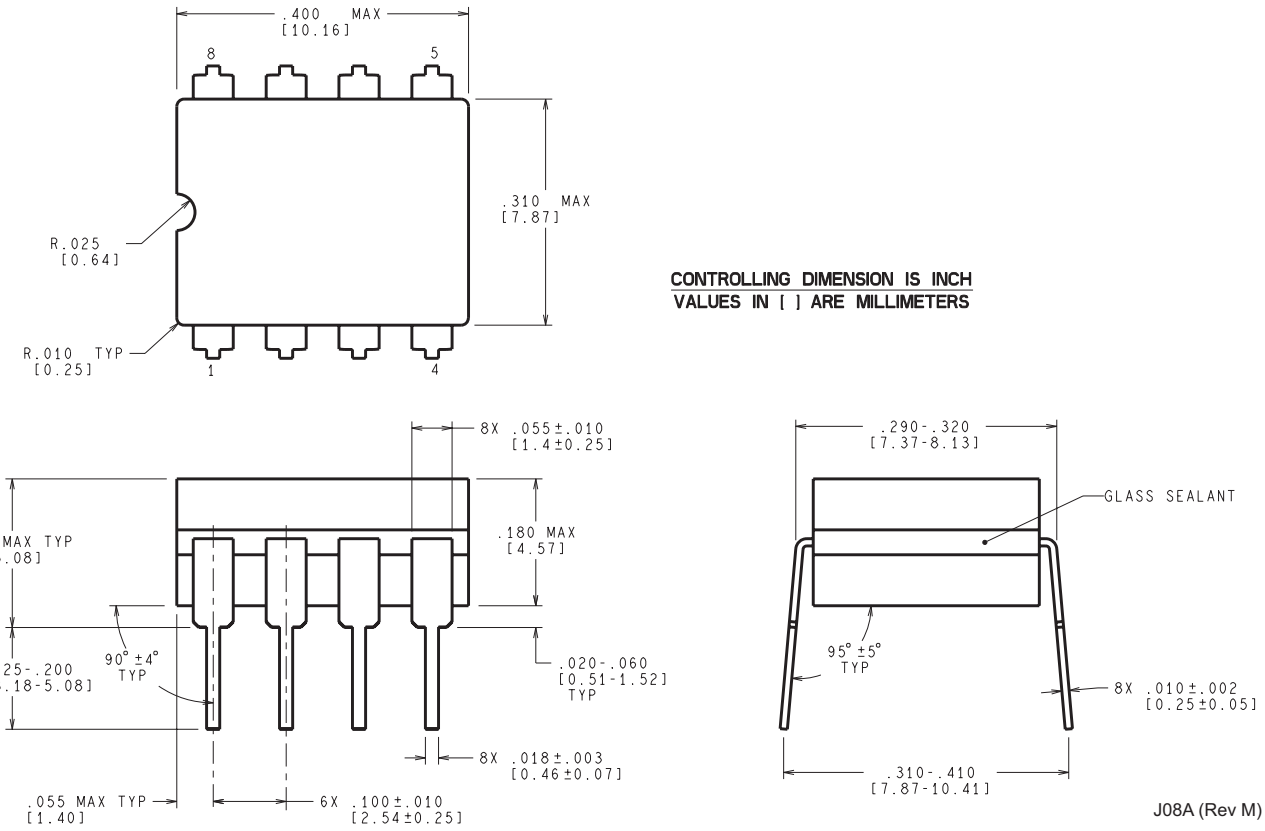
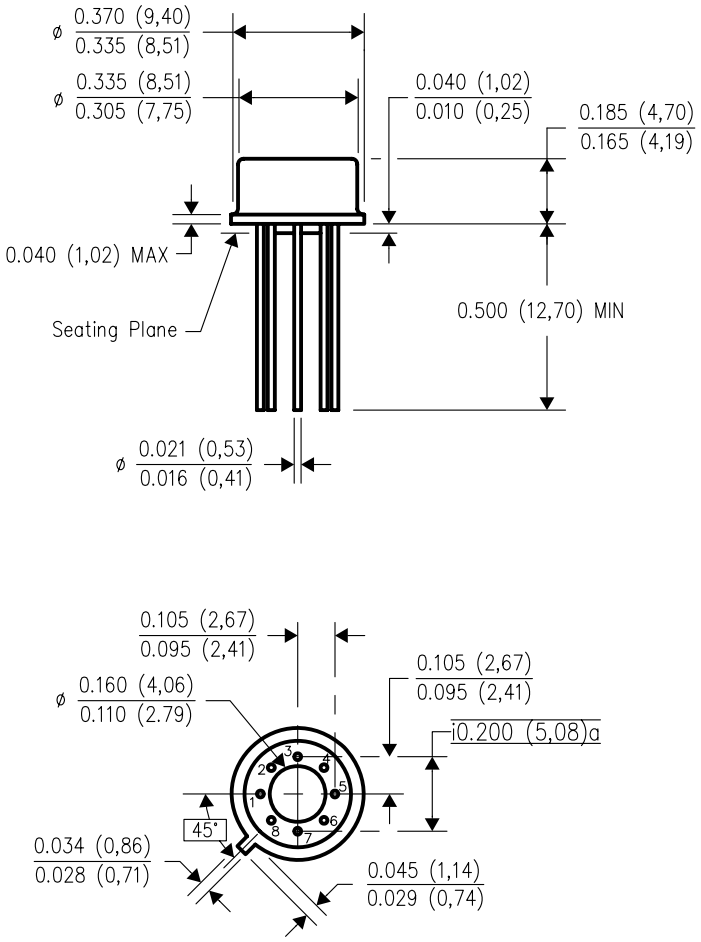

.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

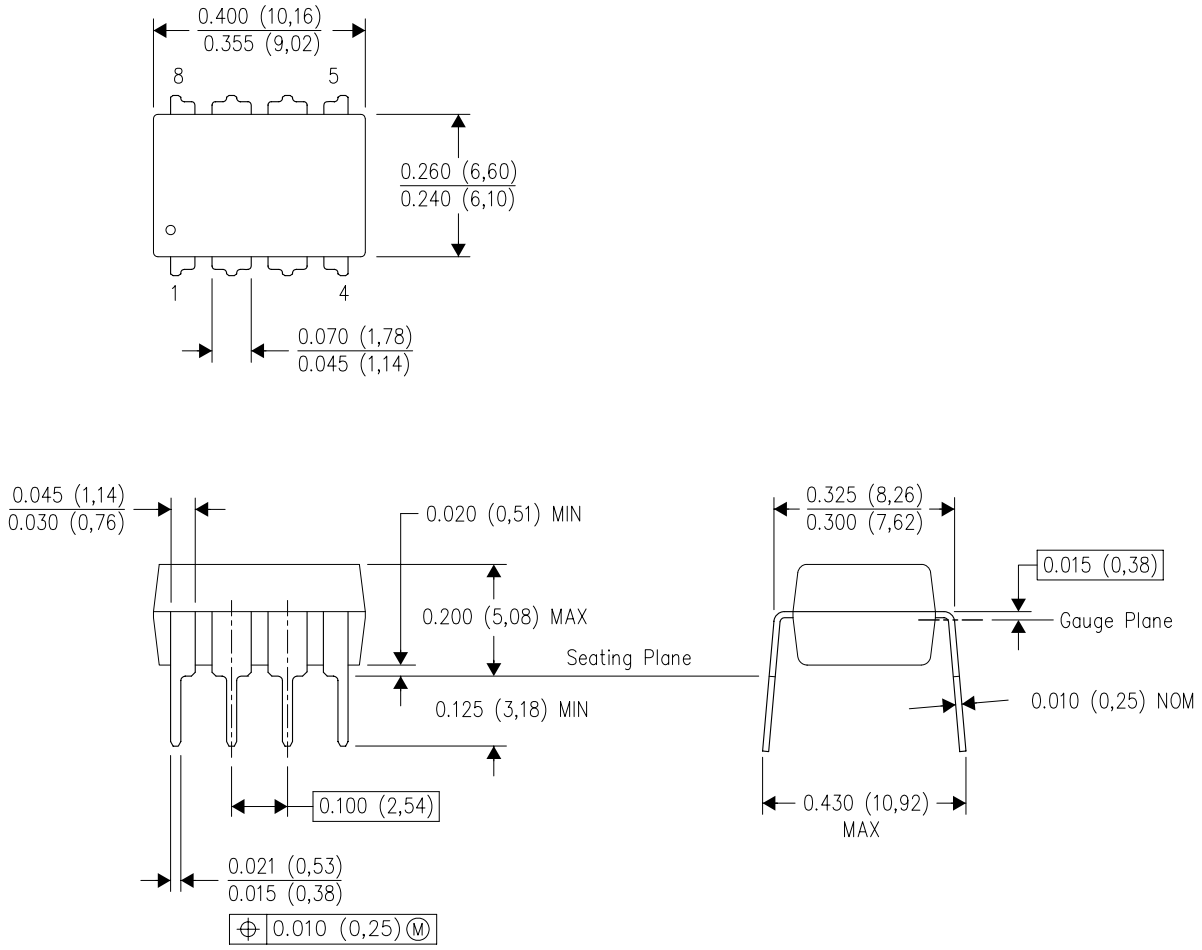
LMC (O–MBCY–W8) METAL CYLINDRICAL PACKAGE



4202483/B 09/07

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO–002/TO–99.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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