



**2N7000  
2N7002**

N-channel 60 V, 1.8  $\Omega$ , 0.35 A, SOT23-3L, TO-92  
STripFET™ Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
2N7000	60 V	< 5 $\Omega$ (@10V)	0.35 A
2N7002	60 V	< 5 $\Omega$ (@10V)	0.20 A

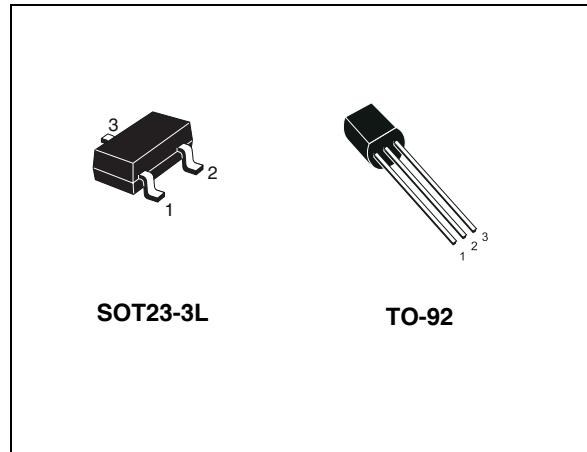
- Low Q<sub>g</sub>
- Low threshold drive

## Application

- Switching applications

## Description

This Power MOSFET is the second generation of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.



**Figure 1. Internal schematic diagram**

**Table 1. Device summary**

Order codes	Marking	Package	Packaging
2N7000	2N7000G	TO-92	Bulk
2N7002	ST2N	SOT23-3L	Tape and reel

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-92	SOT23-3L	
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	60		V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	60		V
$V_{GS}$	Gate- source voltage	$\pm 18$		V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	0.35	0.20	A
$I_{DM}^{(1)}$	Drain current (pulsed)	1.4	1	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	1	0.35	W

1. Pulse width limited by safe operating area

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		TO-92	SOT23-3L	
$R_{thj-amb}$	Thermal resistance junction-ambient max	125	357.1 <sup>(1)</sup>	°C/W
$T_J$	Operating junction temperature	- 55 to 150		°C
$T_{stg}$	Storage temperature			

1. When mounted on 1inch<sup>2</sup> FR-4, 2 Oz copper board.

## 2 Electrical characteristics

( $T_{CASE} = 25^\circ\text{C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0$	60			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{max rating}$ $V_{DS} = \text{max rating}$ , $T_C = 125^\circ\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 18 \text{ V}$			$\pm 100$	nA
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1	2.1	3	V
$R_{DS(\text{on})}$	Static drain-source on resistance	$V_{GS} = 10 \text{ V}, I_D = 0.5 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 0.5 \text{ A}$		1.8 2	5 5.3	$\Omega$ $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10 \text{ V}, I_D = 0.5 \text{ A}$		0.6		s
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$ , $V_{GS} = 0$		43 20 6		pF pF pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 30 \text{ V}, I_D = 0.5 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 4.5 \text{ V}$ (see <a href="#">Figure 16</a> )		5 15 7 8		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 30 \text{ V}, I_D = 1 \text{ A}$ , $V_{GS} = 5 \text{ V}$ (see <a href="#">Figure 17</a> )		1.4 0.8 0.5	2	nC nC nC

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				0.35 1.40	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1 \text{ A}, V_{GS} = 0$			1.2	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 1 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 20 \text{ V}, T_j = 150^\circ\text{C}$ (see <a href="#">Figure 18</a> )		32 25 1.6		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark.

**Table 8. SOT23-3L mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.25
A1	0		0.15
A2	1.00		1.20
A3	0.60		0.70
D	2.826		3.026
E	2.60		3.00
E1	1.526		1.726
e		0.95	
e1		1.90	
L	0.35		0.60
L1		0.59	
L2		0.25	
R	0.05		
R1	0.05		0.20
K	3°		7°
K1	6°		10°

**Figure 23. SOT23-3L drawing**