

## AD8541/AD8542/AD8544

### FEATURES

- Single-Supply Operation: 2.7 V to 5.5 V
- Low Supply Current: 45  $\mu$ A/Amplifier
- Wide Bandwidth: 1 MHz
- No Phase Reversal
- Low Input Currents: 4 pA
- Unity Gain Stable
- Rail-to-Rail Input and Output

### APPLICATIONS

- ASIC Input or Output Amplifier
- Sensor Interface
- Piezo Electric Transducer Amplifier
- Medical Instrumentation
- Mobile Communication
- Audio Output
- Portable Systems

### GENERAL DESCRIPTION

The AD8541/AD8542/AD8544 are single, dual, and quad rail-to-rail input and output single-supply amplifiers featuring very low supply current and 1 MHz bandwidth. All are guaranteed to operate from a 2.7 V single supply as well as a 5 V supply. These parts provide 1 MHz bandwidth at a low current consumption of 45  $\mu$ A per amplifier.

Very low input bias currents enable the AD8541/AD8542/AD8544 to be used for integrators, photodiode amplifiers, piezo electric sensors, and other applications with high source impedance. Supply current is only 45  $\mu$ A per amplifier, ideal for battery operation.

Rail-to-rail inputs and outputs are useful to designers buffering ASICs in single-supply systems. The AD8541/AD8542/AD8544 are optimized to maintain high gains at lower supply voltages, making them useful for active filters and gain stages.

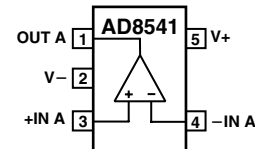
The AD8541/AD8542/AD8544 are specified over the extended industrial temperature range ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ). The AD8541 is available in 8-lead SOIC, 5-lead SC70, and 5-lead SOT-23 packages. The AD8542 is available in 8-lead SOIC, 8-lead MSOP, and 8-lead TSSOP surface-mount packages. The AD8544 is available in 14-lead narrow SOIC and 14-lead TSSOP surface-mount packages. All MSOP, SC70, and SOT versions are available in tape and reel only.

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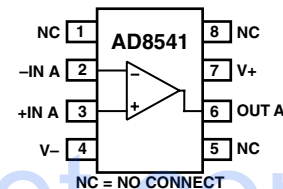
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### PIN CONFIGURATIONS

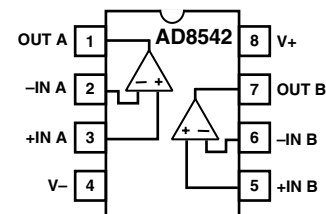
5-Lead SC70 and SOT-23  
(KS and RT Suffixes)



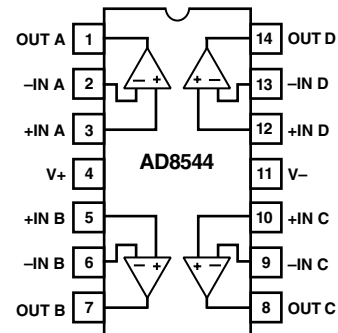
8-Lead SOIC  
(R Suffix)



8-Lead SOIC, MSOP, and TSSOP  
(R, RM, and RU Suffixes)



14-Lead SOIC and TSSOP  
(R and RU Suffixes)



# AD8541/AD8542/AD8544—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS ( $V_S = 2.7\text{ V}$ , $V_{CM} = 1.35\text{ V}$ , $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	6	mV
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		4	7	mV
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			60	pA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.1	100	pA
Input Voltage Range Common-Mode Rejection Ratio	CMRR	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			30	pA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			50	pA
			0		2.7	V
Large Signal Voltage Gain	$A_{VO}$	$V_{CM} = 0\text{ V to } 2.7\text{ V}$	40	45		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	38			dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$R_L = 100\text{ k}\Omega$ , $V_O = 0.5\text{ V to } 2.2\text{ V}$	100	500		V/mV
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	50			V/mV
Bias Current Drift	$\Delta I_B/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2			V/mV
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		4		$\mu\text{V}/^\circ\text{C}$
Offset Current Drift	$\Delta I_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			100	$\text{fA}/^\circ\text{C}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			2,000	$\text{fA}/^\circ\text{C}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.575	2.65		V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.550			V
Output Current	$I_{OUT}$	$V_{OUT} = V_S - 1\text{ V}$		15	100	mV
Closed-Loop Output Impedance	$\pm I_{SC}$ $Z_{OUT}$	$f = 200\text{ kHz}$ , $A_V = 1$		$\pm 20$	125	mV
				50		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 2.5\text{ V to } 6\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	65	76		dB
Supply Current/Amplifier	$I_{SY}$	$V_O = 0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	60	38	55	dB
					75	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 100\text{ k}\Omega$	0.4	0.75		V/ $\mu\text{s}$
Settling Time	$t_s$	To 0.1% (1 V Step)		5		$\mu\text{s}$
Gain Bandwidth Product	GBP			980		kHz
Phase Margin	$\Phi_o$			63		Degrees
<b>NOISE PERFORMANCE</b>						
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		40		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		38		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$			<0.1		$\text{pA}/\sqrt{\text{Hz}}$

Specifications subject to change without notice.

**ELECTRICAL CHARACTERISTICS** ( $V_S = 3.0\text{ V}$ ,  $V_{CM} = 1.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	6	mV
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		4	7	mV
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$			60	pA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			100	pA
Input Voltage Range	Common-Mode Rejection Ratio	$V_{CM} = 0\text{ V to }3\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			1,000	pA
				0.1	30	pA
					50	pA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }3\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			500	pA
				0	3	V
Large Signal Voltage Gain	$A_{VO}$	$R_L = 100\text{ k}\Omega$ , $V_O = 0.5\text{ V to }2.2\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		40	45	dB
				38		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				V/mV
						V/mV
Bias Current Drift	$\Delta I_B/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				V/mV
						$\mu\text{V}/^\circ\text{C}$
Offset Current Drift	$\Delta I_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$				$\text{fA}/^\circ\text{C}$
						$\text{fA}/^\circ\text{C}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.875	2.955		V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.850			V
Output Current	$I_{OUT}$ $\pm I_{SC}$	$V_{OUT} = V_S - 1\text{ V}$		32	100	mV
					125	mV
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 200\text{ kHz}$ , $A_V = 1$		18		mA
				$\pm 25$		mA
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 2.5\text{ V to }6\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	65	76		dB
Supply Current/Amplifier	$I_{SY}$	$V_O = 0\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		40	60	$\mu\text{A}$
					75	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 100\text{ k}\Omega$	0.4	0.8		V/ $\mu\text{s}$
Settling Time	$t_S$	$T_O$ 0.01% (1 V Step)		5		$\mu\text{s}$
Gain Bandwidth Product	GBP			980		kHz
Phase Margin	$\Phi_O$			64		Degrees
<b>NOISE PERFORMANCE</b>						
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		42		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$e_n$	$f = 10\text{ kHz}$		38		$\text{nV}/\sqrt{\text{Hz}}$
					<0.1	$\text{pA}/\sqrt{\text{Hz}}$

Specifications subject to change without notice.

# AD8541/AD8542/AD8544—SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS ( $V_S = 5.0\text{ V}$ , $V_{CM} = 2.5\text{ V}$ , $T_A = 25^\circ\text{C}$ , unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	6	mV
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		4	60	pA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			100	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		0.1	30	pA
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			50	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }5\text{ V}$	40	48		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	38			dB
Large Signal Voltage Gain	$A_{VO}$	$R_L = 100\text{ k}\Omega$ , $V_O = 0.5\text{ V to }2.2\text{ V}$	20	40		V/mV
		$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$	10			V/mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		4		$\mu\text{V}/^\circ\text{C}$
Bias Current Drift	$\Delta I_B/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$		100		fA/ $^\circ\text{C}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		2,000		fA/ $^\circ\text{C}$
Offset Current Drift	$\Delta I_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		25		fA/ $^\circ\text{C}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$I_L = 1\text{ mA}$	4.9	4.965		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.875			V
Output Voltage Low	$V_{OL}$	$I_L = 1\text{ mA}$		25	100	mV
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			125	mV
Output Current	$I_{OUT}$	$V_{OUT} = V_S - 1\text{ V}$		30		mA
	$\pm I_{SC}$			$\pm 60$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 200\text{ kHz}$ , $A_V = 1$		45		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 2.5\text{ V to }6\text{ V}$	65	76		dB
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	60			dB
Supply Current/Amplifier	$I_{SY}$	$V_O = 0\text{ V}$		45	65	$\mu\text{A}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			85	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 100\text{ k}\Omega$ , $C_L = 200\text{ pF}$	0.45	0.92		V/ $\mu\text{s}$
Full-Power Bandwidth	BW <sub>P</sub>	1% Distortion		70		kHz
Settling Time	$t_S$	To 0.1% (1 V Step)		6		$\mu\text{s}$
Gain Bandwidth Product	GBP			1,000		kHz
Phase Margin	$\Phi_o$			67		Degrees
<b>NOISE PERFORMANCE</b>						
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		42		$\text{nV}/\sqrt{\text{Hz}}$
	$e_n$	$f = 10\text{ kHz}$		38		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$			<0.1		$\text{pA}/\sqrt{\text{Hz}}$

Specifications subject to change without notice.

# AD8541/AD8542/AD8544

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

Supply Voltage (V <sub>S</sub> )	6 V
Input Voltage	GND to V <sub>S</sub>
Differential Input Voltage <sup>2</sup>	±6 V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	300°C

### NOTES

<sup>1</sup> Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<sup>2</sup> For supplies less than 6 V, the differential input voltage is equal to ±V<sub>S</sub>.

## PACKAGE INFORMATION

Package Type	θ <sub>JA</sub> *	θ <sub>JC</sub>	Unit
5-Lead SC70 (KS)	376	126	°C/W
5-Lead SOT-23 (RT)	230	146	°C/W
8-Lead SOIC (R)	158	43	°C/W
8-Lead MSOP (RM)	210	45	°C/W
8-Lead TSSOP (RU)	240	43	°C/W
14-Lead SOIC (R)	120	36	°C/W
14-Lead TSSOP (RU)	240	43	°C/W

\*θ<sub>JA</sub> is specified for worst-case conditions, i.e., θ<sub>JA</sub> is specified for device soldered onto a circuit board for surface mount packages.

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding Information
AD8541AKS-R2	-40°C to +125°C	5-Lead SC70	KS-5	A4B
AD8541AKS-REEL7	-40°C to +125°C	5-Lead SC70	KS-5	A4B
AD8541AKSZ-REEL7*	-40°C to +125°C	5-Lead SC70	KS-5	A4B
AD8541AR	-40°C to +125°C	8-Lead SOIC	R-8	
AD8541AR-REEL	-40°C to +125°C	8-Lead SOIC	R-8	
AD8541AR-REEL7	-40°C to +125°C	8-Lead SOIC	R-8	
AD8541ART-R2	-40°C to +125°C	5-Lead SOT-23	RT-5	A4A
AD8541ART-REEL	-40°C to +125°C	5-Lead SOT-23	RT-5	A4A
AD8541ART-REEL7	-40°C to +125°C	5-Lead SOT-23	RT-5	A4A
AD8541ARTZ-REEL*	-40°C to +125°C	5-Lead SOT-23	RT-5	A4A
AD8541ARTZ-REEL7*	-40°C to +125°C	5-Lead SOT-23	RT-5	A4A
AD8542AR	-40°C to +125°C	8-Lead SOIC	R-8	
AD8542AR-REEL	-40°C to +125°C	8-Lead SOIC	R-8	
AD8542AR-REEL7	-40°C to +125°C	8-Lead SOIC	R-8	
AD8542ARZ*	-40°C to +125°C	8-Lead SOIC	R-8	
AD8542ARZ-REEL*	-40°C to +125°C	8-Lead SOIC	R-8	
AD8542ARZ-REEL7*	-40°C to +125°C	8-Lead SOIC	R-8	
AD8542ARM-R2	-40°C to +125°C	8-Lead MSOP	RM-8	AVA
AD8542ARM-REEL	-40°C to +125°C	8-Lead MSOP	RM-8	AVA
AD8542ARU	-40°C to +125°C	8-Lead TSSOP	RU-8	
AD8542ARU-REEL	-40°C to +125°C	8-Lead TSSOP	RU-8	
AD8542ARUZ*	-40°C to +125°C	8-Lead TSSOP	RU-8	
AD8542ARUZ-REEL*	-40°C to +125°C	8-Lead TSSOP	RU-8	
AD8544AR	-40°C to +125°C	14-Lead SOIC	R-14	
AD8544AR-REEL	-40°C to +125°C	14-Lead SOIC	R-14	
AD8544AR-REEL7	-40°C to +125°C	14-Lead SOIC	R-14	
AD8544ARZ*	-40°C to +125°C	14-Lead SOIC	R-14	
AD8544ARZ-REEL*	-40°C to +125°C	14-Lead SOIC	R-14	
AD8544ARZ-REEL7*	-40°C to +125°C	14-Lead SOIC	R-14	
AD8544ARU	-40°C to +125°C	14-Lead TSSOP	RU-14	
AD8544ARU-REEL	-40°C to +125°C	14-Lead TSSOP	RU-14	
AD8544ARUZ*	-40°C to +125°C	14-Lead TSSOP	RU-14	
AD8544ARUZ-REEL*	-40°C to +125°C	14-Lead TSSOP	RU-14	

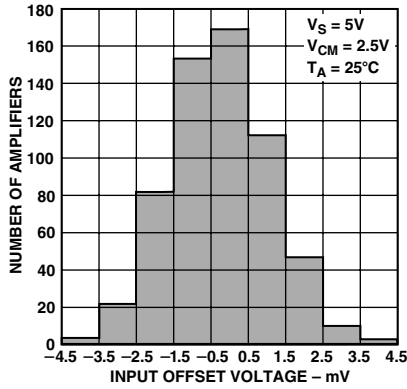
\*Z = Pb-free part.

### ESD CAUTION

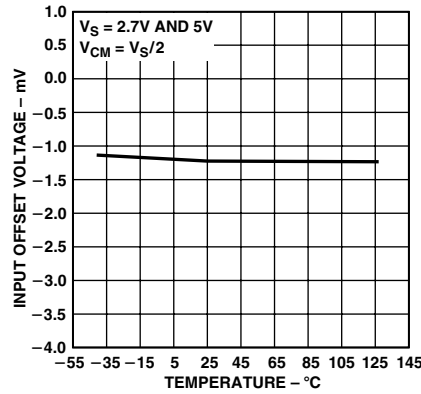
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8541/AD8542/AD8544 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



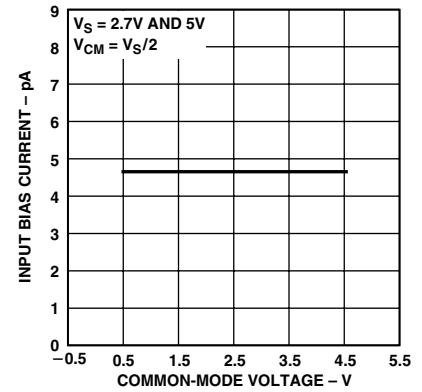
# AD8541/AD8542/AD8544—Typical Performance Characteristics



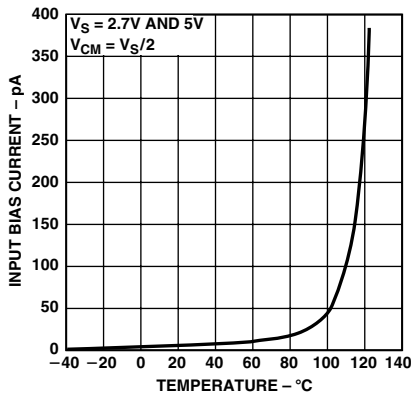
TPC 1. Input Offset Voltage Distribution



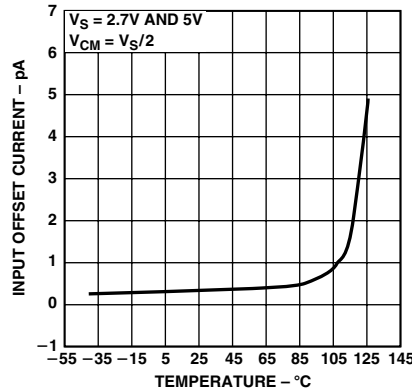
TPC 2. Input Offset Voltage vs. Temperature



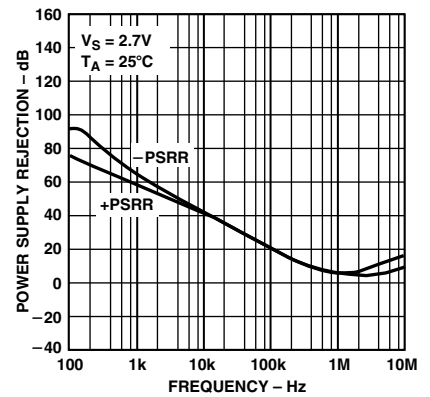
TPC 3. Input Bias Current vs. Common-Mode Voltage



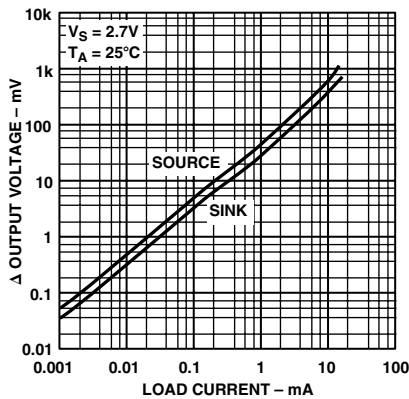
TPC 4. Input Bias Current vs. Temperature



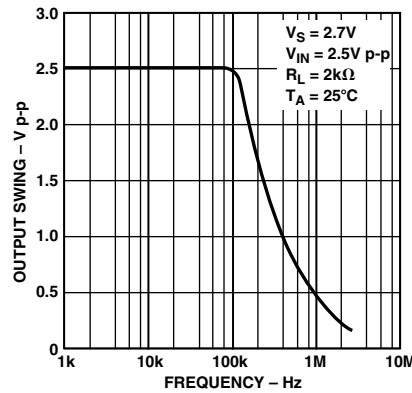
TPC 5. Input Offset Current vs. Temperature



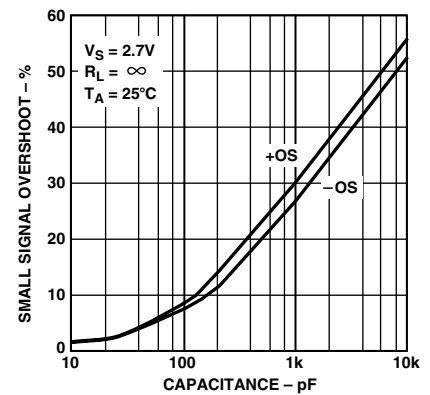
TPC 6. Power Supply Rejection Ratio vs. Frequency



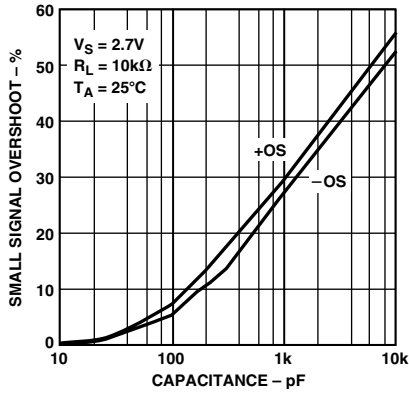
TPC 7. Output Voltage to Supply Rail vs. Load Current



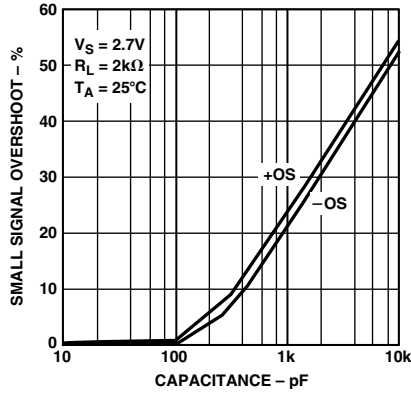
TPC 8. Closed-Loop Output Voltage Swing vs. Frequency



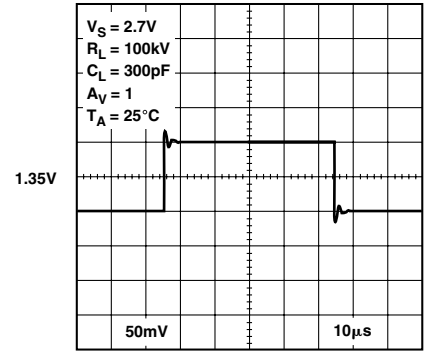
TPC 9. Small Signal Overshoot vs. Load Capacitance



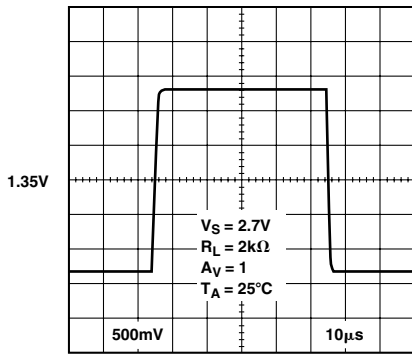
TPC 10. Small Signal Overshoot vs. Load Capacitance



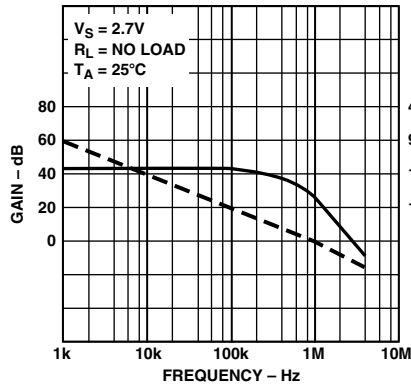
TPC 11. Small Signal Overshoot vs. Load Capacitance



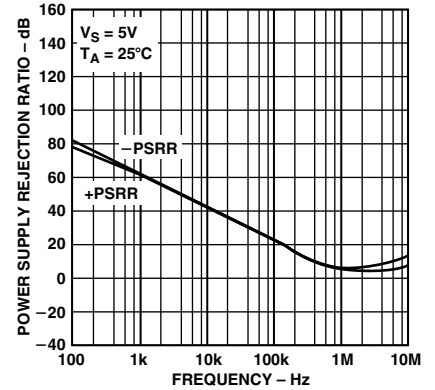
TPC 12. Small Signal Transient Response



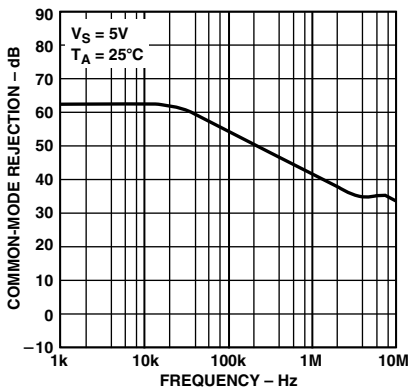
TPC 13. Large Signal Transient Response



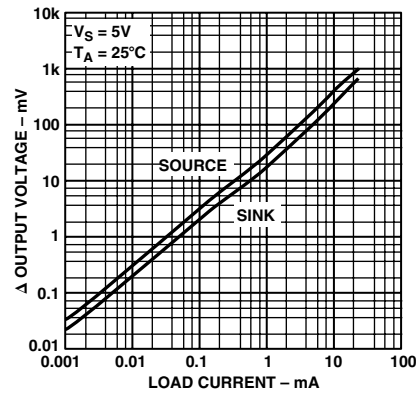
TPC 14. Open-Loop Gain and Phase vs. Frequency



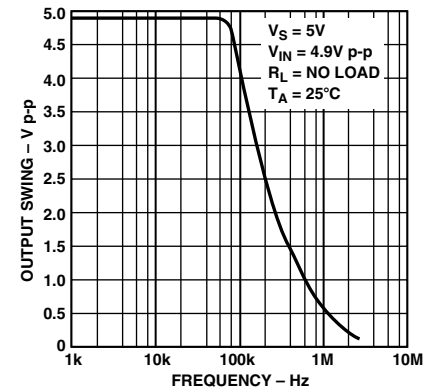
TPC 15. Power Supply Rejection Ratio vs. Frequency



TPC 16. Common-Mode Rejection Ratio vs. Frequency

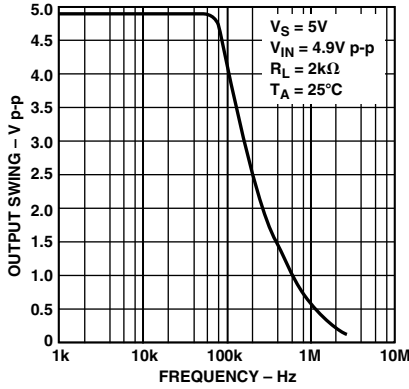


TPC 17. Output Voltage to Supply Rail vs. Frequency

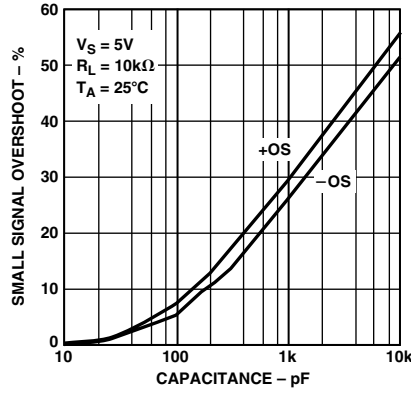


TPC 18. Closed-Loop Output Voltage Swing vs. Frequency

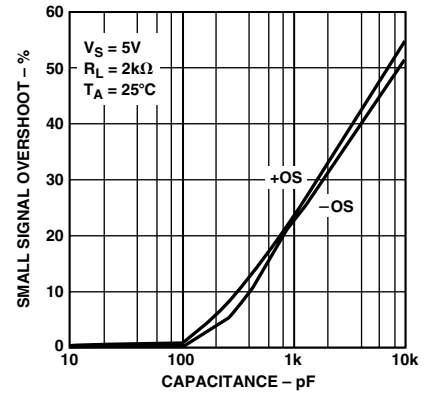
# AD8541/AD8542/AD8544



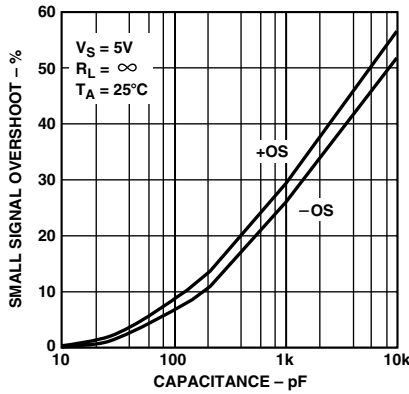
TPC 19. Closed-Loop Output Voltage Swing vs. Frequency



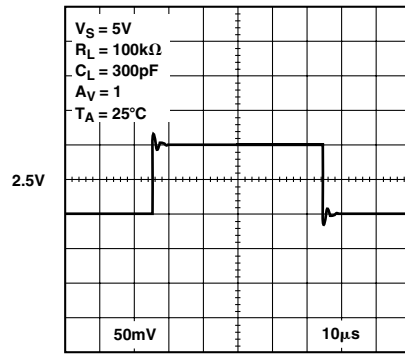
TPC 20. Small Signal Overshoot vs. Load Capacitance



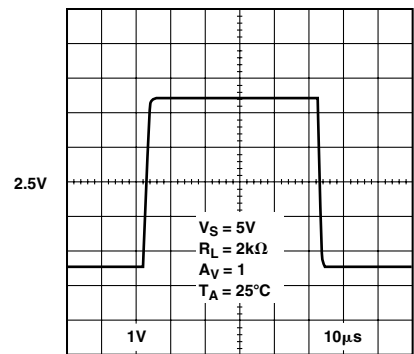
TPC 21. Small Signal Overshoot vs. Load Capacitance



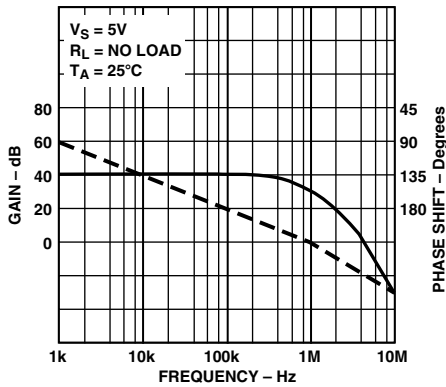
TPC 22. Small Signal Overshoot vs. Load Capacitance



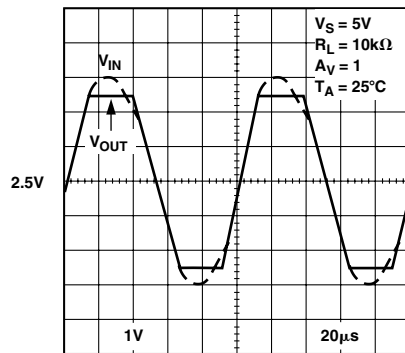
TPC 23. Small Signal Transient Response



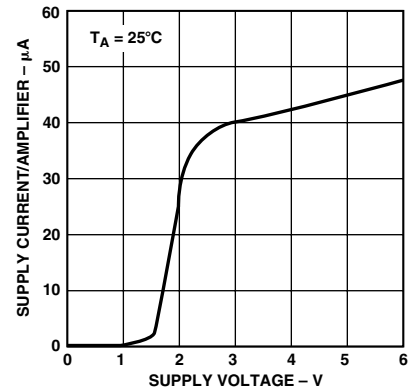
TPC 24. Large Signal Transient Response



TPC 25. Open-Loop Gain and Phase vs. Frequency

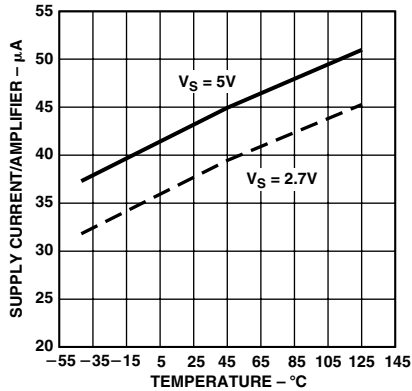


TPC 26. No Phase Reversal

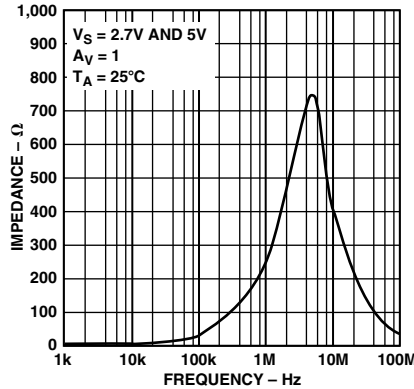


TPC 27. Supply Current per Amplifier vs. Supply Voltage

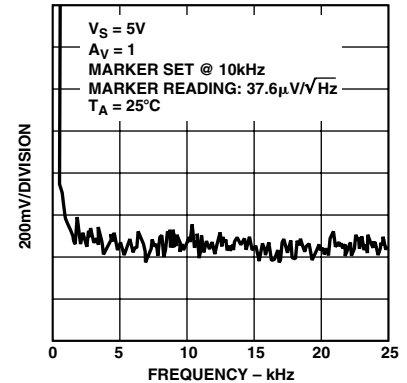




TPC 28. Supply Current per Amplifier vs. Temperature



TPC 29. Closed-Loop Output Impedance vs. Frequency



TPC 30. Voltage Noise

## NOTES ON THE AD854x AMPLIFIERS

The AD8541/AD8542/AD8544 amplifiers are improved performance general-purpose operational amplifiers. Performance has been improved over previous amplifiers in several ways.

### Lower Supply Current for 1 MHz Gain Bandwidth

The AD854x series typically uses 45 μA of current per amplifier. This is much less than the 200 μA to 700 μA used in earlier generation parts with similar performance. This makes the AD854x series a good choice for upgrading portable designs for longer battery life. Alternatively, additional functions and performance can be added at the same current drain.

### Higher Output Current

At 5 V single supply, the short-circuit current is typically 60 μA. Even 1 V from the supply rail, the AD854x amplifiers can provide 30 mA, sourcing or sinking.

Sourcing and sinking are strong at lower voltages, with 15 mA available at 2.7 V and 18 mA at 3.0 V. For even higher output currents, please see the Analog Devices AD8531/AD8532/AD8534 parts, with output currents to 250 mA. Information on these parts is available from your Analog Devices representative, and data sheets are available at the Analog Devices website at [www.analog.com](http://www.analog.com).

### Better Performance at Lower Voltages

The AD854x family of parts has been designed to provide better ac performance, at 3.0 V and 2.7 V, than previously available parts. Typical gain-bandwidth product is close to 1 MHz at 2.7 V. Voltage gain at 2.7 V and 3.0 V is typically 500,000. Phase margin is typically over 60°, making the part easy to use.

## APPLICATIONS

### Notch Filter

The AD8542 has very high open-loop gain (especially with a supply voltage below 4 V), which makes it useful for active filters of all types. For example, Figure 1 illustrates the AD8542 in the classic Twin-T Notch Filter design. The Twin-T Notch is desired for simplicity, low output impedance, and minimal use of op amps. In fact, this notch filter may be designed with only one op amp if Q adjustment is not required. Simply remove U2 as illustrated in Figure 2. However, a major drawback to this circuit topology is ensuring that all the Rs and Cs closely match. The components must closely match or notch frequency offset and

drift will cause the circuit to no longer attenuate at the ideal notch frequency. To achieve desired performance, 1% or better component tolerances or special component screens are usually required. One method to desensitize the circuit-to-component mismatch is to increase R2 with respect to R1, which lowers Q. A lower Q increases attenuation over a wider frequency range but reduces attenuation at the peak notch frequency.

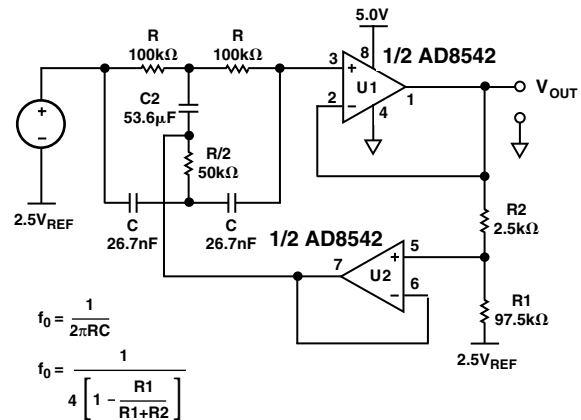


Figure 1. 60 Hz Twin-T Notch Filter, Q = 10

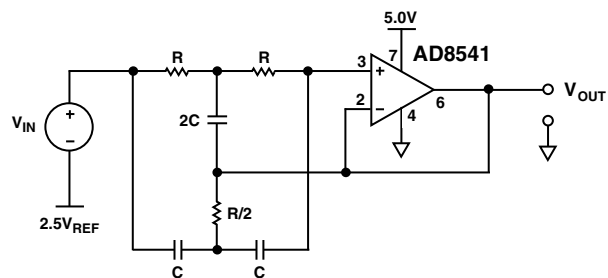


Figure 2. 60 Hz Twin-T Notch Filter, Q = ∞ (Ideal)

Figure 3 shows another example of the AD8542 in a notch filter circuit. The FNDR notch filter has fewer critical matching requirements than the Twin-T Notch and for the FNDR Q is directly proportional to a single resistor R1. While matching component values is still important, it is also

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much easier and/or less expensive to accomplish in the FNDR circuit. For example, the Twin-T notch uses three capacitors with two unique values, whereas the FNDR circuit uses only two capacitors, which may be of the same value. U3 is simply a buffer that is added to lower the output impedance of the circuit.

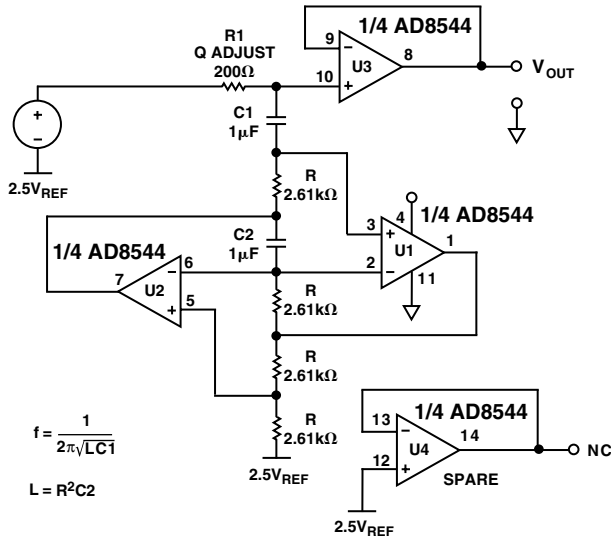


Figure 3. FNDR 60 Hz Notch Filter with Output Buffer

## Comparator Function

A comparator function is a common application for a spare op amp in a quad package. Figure 4 illustrates 1/4 of the AD8544 as a comparator in a standard overload detection application. Unlike many op amps, the AD854x family can double as comparators because this op amp family has rail-to-rail differential input range, rail-to-rail output, and a great speed versus power ratio. R2 is used to introduce hysteresis. The AD854x, when used as comparators, have 5 μs propagation delay at 5 V and 5 μs overload recovery time.

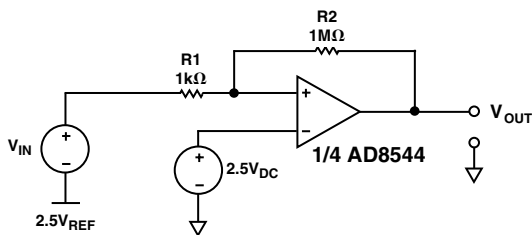


Figure 4. AD854x Comparator Application—Overload Detector

## Photodiode Application

The AD854x family has very high impedance with input bias current typically around 4 pA. This characteristic allows the AD854x op amps to be used in photodiode applications and other applications that require high input impedance. Note that the AD854x has significant voltage offset, which can be removed by capacitive coupling or software calibration.

Figure 5 illustrates a photodiode or current measurement application. The feedback resistor is limited to 10 MΩ to avoid excessive output offset. Also, note that a resistor is not needed on the noninverting input to cancel bias current offset because the bias current related output offset is not significant when compared to the voltage offset contribution. For the best performance follow the standard high impedance layout techniques including:

- Shield the circuit.
- Clean the circuit board.
- Put a trace connected to the noninverting input around the inverting input.
- Use separate analog and digital power supplies.

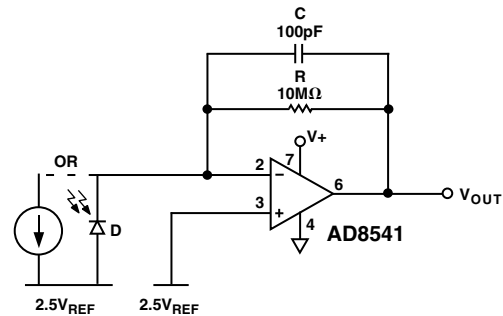


Figure 5. High Input Impedance Application—Photodiode Amplifier

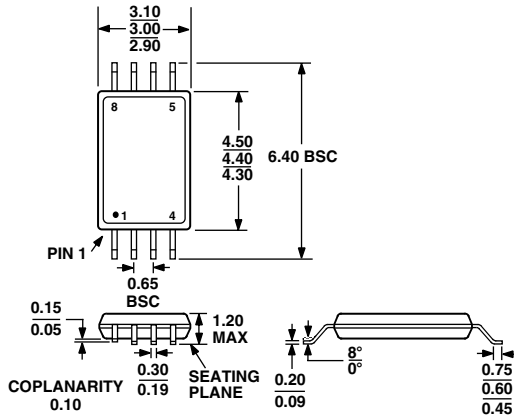


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## OUTLINE DIMENSIONS

### 8-Lead Thin Shrink Small Outline Package [TSSOP] (RU-8)

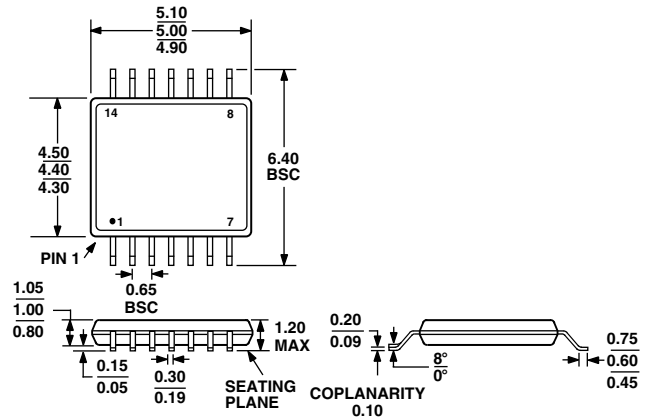
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AA

### 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

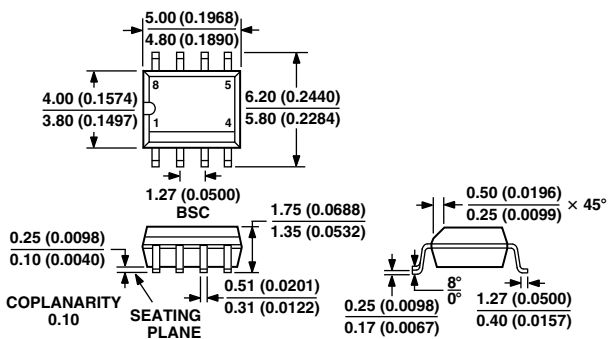
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AB-1

### 8-Lead Standard Small Outline Package [SOIC] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

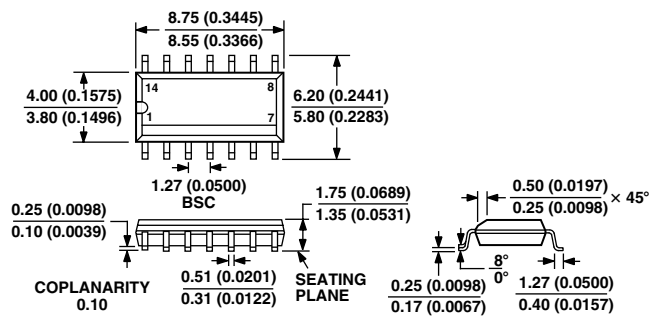


COMPLIANT TO JEDEC STANDARDS MS-012AA

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### 14-Lead Standard Small Outline Package [SOIC] Narrow Body (R-14)

Dimensions shown in millimeters and (inches)



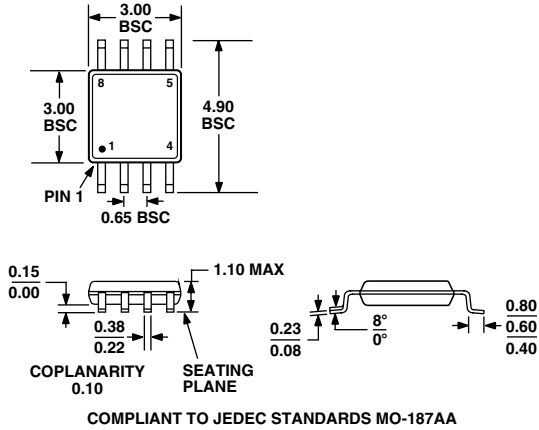
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CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

## OUTLINE DIMENSIONS

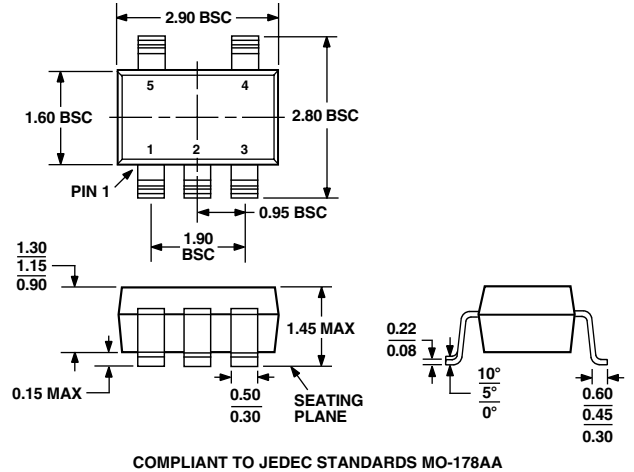
### 8-Lead Mini Small Outline Package [MSOP] (RM-8)

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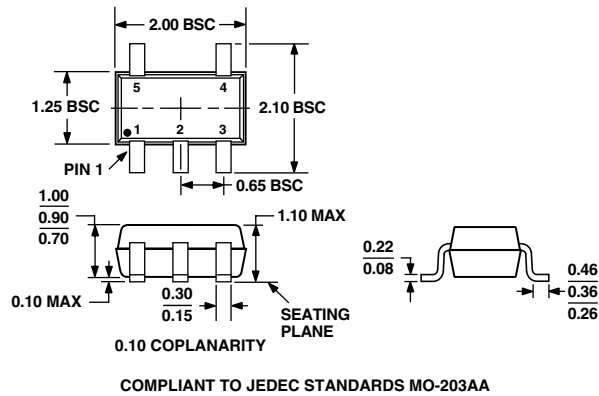
### 5-Lead Small Outline Transistor Package [SOT-23] (RT-5)

Dimensions shown in millimeters



### 5-Lead Thin Shrink Small Outline Transistor Package [SC70] (KS-5)

Dimensions shown in millimeters



# AD8541/AD8542/AD8544

## Revision History

<b>Location</b>	<b>Page</b>
<b>8/04—Data Sheet changed from REV. C to REV. D.</b>	
Changes to ORDERING GUIDE .....	5
Change to Figure 3 .....	10
Updated OUTLINE DIMENSIONS .....	12
<b>1/03—Data Sheet changed from REV. B to REV. C.</b>	
Updated format .....	Universal
Change to GENERAL DESCRIPTION .....	1
Changes to ORDERING GUIDE .....	5
Changes to OUTLINE DIMENSIONS .....	12



