TOPAZ SEMICONDUCTOR

SD304, SD306

N-CHANNEL ENHANCEMENT-MODE DUAL GATE D-MOS FET

ORDERING INFORMATION

Sorted Chips in Waffle Pack	SD304CHP	SD306CHP
TO-206AF (TO-72) Package	SD304DE	SD306DE
Shorting Rings	SD304DE/R	SD306DE/R

FEATURES

- Normally Off-Enhancement-Mode Operation
- Dual Gate with Gate Protective Diodes
- Low Feedback Capacitance — c_{rss} .03pF (typ)
- Wide Dynamic Range-Remote AGC capability
- High Power Gain- 17dB min. @ 500MHz (SD306)
- Low Noise-6.0dB max. @ 500MHz (SD306)
- Low Cross-Modulation Distortion

APPLICATIONS

- Wide Band (Unneutralized) VHF/UHF Amplifiers
- VHF/UHF Linear Mixers

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

V_{DS} Drain-Source Voltage
- SD304 ..... +25V
- SD306 ..... +20V

V_{G1B} Gate 1-Substrate Voltage
- SD304 ..... −0.3 to +10V
- SD306 ..... −0.3 to +20V

V_{G2B} Gate 2-Substrate Voltage
- SD304 ..... −0.3 to +15V
- SD306 ..... −0.3 to +20V

I_D Continuous Drain Current (Note 1) 50mA

P_D Continuous Power Dissipation (Note 1)
- T_A = +25°C (Free Air) 300mW
- T_C = +25°C (Infinite Heat Sink) 1.2W

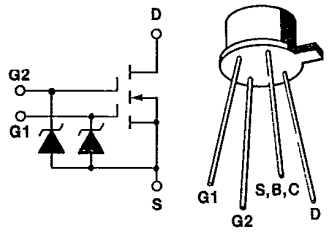
Power Derating Factors (Note 1)
- Free Air ..... 3.0mW/°C
- Infinite Heat Sink ..... 12mW/°C

T_{op} Operating Junction Temperature Range ..... −55 to +125°C

T_{stg} Storage Temperature Range .. −65 to +175°C

Note 1: Not applicable to chips. Final value depends mounting substrate.

SCHEMATIC DIAGRAM

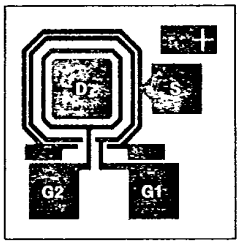


Pin 1-Drain, 2-Gate 2
Pin 3-Gate 1,
Pin 4-Source, Substrate, Case

PACKAGE DIMENSIONS (TO-72) TO-206AF

(See Package 3)

CHIP CONFIGURATION



Chip backside connected to source
Dimensions: .022 x .022 x .013 inches

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ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

#		PARAMETER	SD304 MIN	SD304 TYP	SD304 MAX	SD306 MIN	SD306 TYP	SD306 MAX	UNIT	TEST CONDITIONS
1	STATIC	BV_{DS} Drain-Source Breakdown Voltage	25	30		20	25		V	$I_D = 5\mu A$, $V_{G1S} = V_{G2S} = 0$
2	STATIC	I_{DSS} Drain-Source OFF Leakage Current		.01	1.0		.01	1.0	μA	$V_{DS} = 15V$, $V_{G1S} = V_{G2S} = 0$
3	STATIC	I_{G1SS} Gate 1 Leakage Current		1.0	100		1.0	100	nA	$V_{G1S} = 5V$, $V_{G2S} = V_{DS} = 0$
4	STATIC	I_{G2SS} Gate 2 Leakage Current		1.0	100		1.0	100	nA	$V_{G2S} = 10V$, $V_{G1S} = V_{DS} = 0$
5	STATIC	V_{T1} Gate 1-Source Threshold Voltage	0.1	1.0	2.0	0.1	0.5	1.5	V	$V_{DS} = V_{G1S}$, $V_{G2S} = 10V$, $I_D = 1\mu A$
6	STATIC	V_{T2} Gate 2-Source Threshold Voltage	0.1	1.0	2.0				V	$V_{G1S} = 4V$; $V_{DS} = V_{G2S}$, $I_D = 1\mu A$
7	STATIC	V_{T2} Gate 2-Source Threshold Voltage				0.1	0.5	1.5	V	$V_{G1S} = 5V$; $V_{DS} = V_{G2S}$, $I_D = 1\mu A$
8	STATIC	$r_{DS(on)}$ Drain-Source ON Resistance		90	130		65	100	ohms	$I_D = 1mA$, $V_{G1S} = 5V$, $V_{G2S} = 10V$
9	DYNAMIC	g_{fs} Common-Source Forward Transconductance	8.0	10		13	15		mmhos	$V_{DS} = 15V$, $I_D = 18mA$, $V_{G2S} = 10V$, f = 1KHz
10	DYNAMIC	c_{lss} Common-Source Input Capacitance		2.5	3.0		3.3	3.6	pF	$V_{DS} = 15V$, $I_D = 18mA$, $V_{G2S} = 10V$, f = 1MHz
11	DYNAMIC	c_{oss} Common-Source Output Capacitance		1.0	1.2		1.0	1.3	pF	$V_{DS} = 15V$, $V_{G1S} = 0$, $V_{G2S} = 10V$, f = 1MHz
12	DYNAMIC	c_{rss} Common-Source Reverse Transfer Capacitance		.03			.03		pF	$V_{DS} = 15V$, $V_{G1S} = 0$, $V_{G2S} = 10V$, f = 1MHz
13	DYNAMIC	Re(Y11) Input Admittance					1.11		mmhos	$V_{DS} = 15V$, $I_D = 18mA$, $V_{G2S} = 10V$, f = 200MHz
14	DYNAMIC	Im(Y11) Input Admittance					4.76		mmhos	$V_{DS} = 15V$, $I_D = 18mA$, $V_{G2S} = 10V$, f = 200MHz

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ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

PARAMETER		SD304			SD306			UNIT	TEST CONDITIONS	
		MIN	TYP	MAX	MIN	TYP	MAX			
Re (Y22)	Output Admittance					1.05		mmhos	V_{DS} = 15V, I_D = 18mA V_{G2S} = 10V, f = 200MHz	
Im (Y22)						1.54		mmhos		
Re (Y21)	Forward Transmittance					13.23		mmhos		
Im (Y21)						−5.62		mmhos		
Re (Y12)	Reverse Transmittance					0.01		mmhos		
Im (Y12)						−0.04		mmhos		
G_{ps}	Power Gain	13	16					dB	f = 500MHz	V_{DS} = 15V V_{G2S} = 10V I_D = 18mA
					17	20		dB	f = 200MHz	
NF	Noise Figure		5.0	6.0				dB	f = 500MHz	
						1.5	2.5	dB	f = 200MHz	
AGC (V_{G2S})	Range of Automatic Gain Control		40					dB	V_{G1S} ≅ 3.5V f = 500MHz	V_{DS} = 15V V_{G2S} = 10V to 0V
						50		dB	V_{G1S} ≅ 2.5V f = 200MHz	
E_{INT}	Interfering Signal at Gate for 1% Cross-Modulation Distortion (Peak Voltage ref. to 50 ohm system)		200					mV	fo = 500MHz fi = 501MHz	V_{DS} = 15V V_{G2S} = 10V I_D = 18mA
						480		mV	fo = 200MHz fi = 196MHz	
G_{psc}	Conversion Power Gain (I_D = 8mA)				14	17		dB	V_{DS} = 15V, V_{G1S} = V_{G2S} frf = 200MHz, f1 = 245MHz	