

## Kinetis KV31F 512KB Flash

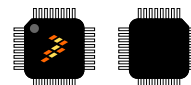
120 MHz ARM® Cortex®-M4 Based Microcontroller with FPU

The KV31 MCU family is a highly scalable member of the Kinetis V series and provides a high-performance, cost-competitive motor control solution. Built on the ARM® Cortex®-M4 core running at 120 MHz, combined with floating point and DSP capability, it delivers a highly capable platform enabling customers to build a highly scalable solution portfolio.

Additional features include:

- Dual 16-bit ADCs sampling at up to 1.2 MS/s in 12-bit mode
- 20 channels of highly flexible motor control timers (PWMs) across 4 independent time bases
- Large RAM block enabling local execution of fast control loops at full clock speed
- Enabled to support Kinetis Motor Suite (KMS), a bundled hardware and software solution that enables rapid configuration of BLDC and PMSM motor drive systems

**MKV31F512VLL12**  
**MKV31F512VLH12**  
**MKV31F512VLL12P**



100 & 64 LQFP(LL&LH)  
14x14x1.4 mm P .5(LL) 10x10x1.4 mm P .5(LH)

Searchdatasheet.com

### Performance

- 120 MHz ARM Cortex-M4 core with DSP instructions delivering 1.25 Dhrystone MIPS per MHz

### Memories and memory interfaces

- 512 KB of embedded flash and 96 KB of RAM
- FlexBus external bus interface
- Preprogrammed Kinetis flashloader for one-time, in-system factory programming

### Timers

- Two 8-ch motor-control/general purpose/PWM timers
- Two 2-ch motor-control/general purpose timers with quadrature decoder functionality

### Security and integrity modules

- Hardware CRC module
- 128-bit unique identification (ID) number per chip
- Hardware random-number generator
- Flash access control to protect proprietary software

### Human-machine interface

- Up to 70 general-purpose I/O (GPIO)

### Operating Characteristics

### Analog modules

- Two 16-bit SAR ADCs (1.2 MS/s in 12bit mode)
- Two 12-bit DACs
- Two analog comparators (CMP) with 6-bit DAC
- Accurate internal voltage reference

### System peripherals

- 16-channel DMA controller
- Independent external and software watchdog monitor

### Clocks

- One crystal oscillator with two ranges: 32-40 kHz or 3-32 MHz
- Three internal oscillators: 32 kHz, 4 MHz, & 48 MHz
- Multipurpose clock generator with PLL and FLL

### Communication interfaces

- Two SPI modules
- Three UART modules and one low-power UART
- Two I2C: Support for up to 1 Mbps operation

### Kinetis Motor Suite

- Supports Velocity and Position control of BLDC & PMSM motors

- Voltage range (including flash writes): 1.71 to 3.6 V
- Temperature range (ambient): -40 to 105°C
- Implements Field Orient Control (FOC) using Back EMF to improve motor efficiency
- Utilizes SpinTAC control theory that improves overall system performance and reliability

### Ordering Information

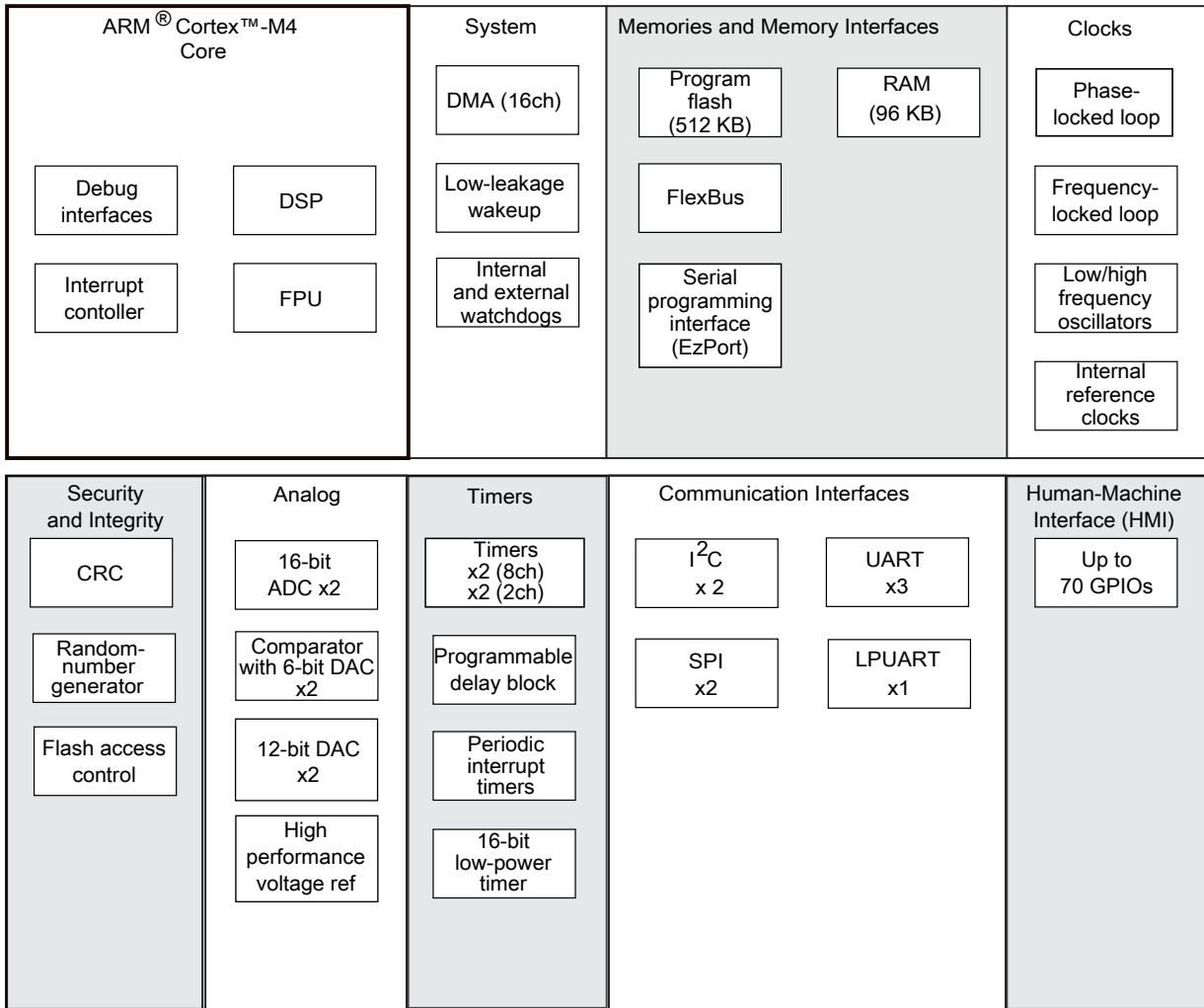
Part Number	Memory		Maximum number of I/O's
	Flash (KB)	SRAM (KB)	
MKV31F512VLL12	512	96	70
MKV31F512VLH12	512	96	46
MKV31F512VLL12P	504	96	70

### Related Resources

Type	Description	Document
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector	<a href="#">Product Selector</a>
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	<a href="#">KV30FKV31FPB</a>
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	<a href="#">KV31P100M120SF7RM</a>
Data Sheet	The Data Sheet is this document. It includes electrical characteristics and signal connections.	<a href="#">KV31P100M120SF7</a>
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	<a href="#">KINETIS_xN50M<sup>1</sup></a>
KMS User Guide	The KMS User Guide provides a comprehensive description of the features and functions of the Kinetis Motor Suite solution.	<a href="#">Kinetis Motor Suite User's Guide (KMS100UG)<sup>2</sup></a>
KMS API Reference Manual	The KMS API reference manual provides a comprehensive description of the API of the Kinetis Motor Suite function blocks.	<a href="#">Kinetis Motor Suite API Reference Manual (KMS100RM)<sup>2</sup></a>
Package drawing	Package dimensions are provided by part number: <ul style="list-style-type: none"> <li>• MKV31F512VLL12</li> <li>• MKV31F512VLH12</li> <li>• MKV31F512VLL12P</li> </ul>	Package drawing: <ul style="list-style-type: none"> <li>• <a href="#">98ASS23308W</a></li> <li>• <a href="#">98ASS23234W</a></li> <li>• <a href="#">98ASS23308W</a></li> </ul>

1. To find the associated resource, go to [freescale.com](#) and perform a search using this term with the x replaced by the revision of the device you are using.
2. To find the associated resource, go to [freescale.com](#) and perform a search using Document ID

Figure 1 shows the functional modules in the chip.



**Figure 1. Functional block diagram**

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# 1 Ratings

## 1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>STG</sub>	Storage temperature	-55	150	°C	1
T <sub>SDR</sub>	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

## 1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>HBM</sub>	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V <sub>CDM</sub>	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I <sub>LAT</sub>	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 1.4 Voltage and current operating ratings

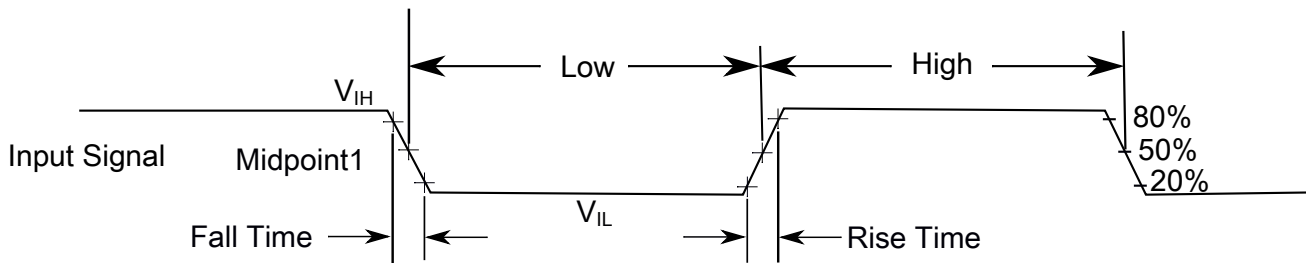
Symbol	Description	Min.	Max.	Unit
$V_{DD}$	Digital supply voltage	-0.3	3.8	V
$I_{DD}$	Digital supply current	—	169	mA
$V_{DIO}$	Digital input voltage	-0.3	$V_{DD} + 0.3$	V
$V_{AIO}$	Analog <sup>1</sup>	-0.3	$V_{DD} + 0.3$	V
$I_D$	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

## 2 General

### 2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is  $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

### 2.2 Nonswitching electrical specifications

#### 2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	3.6	V	

Table continues on the next page...

**Table 1. Voltage and current operating requirements (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>DDA</sub>	Analog supply voltage	1.71	3.6	V	
V <sub>DD</sub> – V <sub>DDA</sub>	V <sub>DD</sub> -to-V <sub>DDA</sub> differential voltage	–0.1	0.1	V	
V <sub>SS</sub> – V <sub>SSA</sub>	V <sub>SS</sub> -to-V <sub>SSA</sub> differential voltage	–0.1	0.1	V	
V <sub>IH</sub>	Input high voltage <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V</li> <li>• 1.7 V ≤ V<sub>DD</sub> ≤ 2.7 V</li> </ul>	0.7 × V <sub>DD</sub>	—	V	
		0.75 × V <sub>DD</sub>	—	V	
V <sub>IL</sub>	Input low voltage <ul style="list-style-type: none"> <li>• 2.7 V ≤ V<sub>DD</sub> ≤ 3.6 V</li> <li>• 1.7 V ≤ V<sub>DD</sub> ≤ 2.7 V</li> </ul>	—	0.35 × V <sub>DD</sub>	V	
		—	0.3 × V <sub>DD</sub>	V	
V <sub>HYS</sub>	Input hysteresis	0.06 × V <sub>DD</sub>	—	V	
I <sub>ICIO</sub>	Analog and I/O pin DC injection current — single pin <ul style="list-style-type: none"> <li>• V<sub>IN</sub> &lt; V<sub>SS</sub>-0.3V (Negative current injection)</li> </ul>	-3	—	mA	1
I <sub>ICcont</sub>	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins <ul style="list-style-type: none"> <li>• Negative current injection</li> </ul>	-25	—	mA	
V <sub>ODPU</sub>	Open drain pullup voltage level	V <sub>DD</sub>	V <sub>DD</sub>	V	2
V <sub>RAM</sub>	V <sub>DD</sub> voltage required to retain RAM	1.2	—	V	

1. All analog and I/O pins are internally clamped to V<sub>SS</sub> through ESD protection diodes. If V<sub>IN</sub> is less than V<sub>IO\_MIN</sub> or greater than V<sub>IO\_MAX</sub>, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R=(V<sub>IO\_MIN</sub>-V<sub>IN</sub>)/|I<sub>ICIO</sub>|.
2. Open drain outputs must be pulled to V<sub>DD</sub>.

## 2.2.2 LVD and POR operating requirements

**Table 2. V<sub>DD</sub> supply LVD and POR operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>POR</sub>	Falling V <sub>DD</sub> POR detect voltage	0.8	1.1	1.5	V	
V <sub>LVDH</sub>	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V <sub>LVW1H</sub> V <sub>LVW2H</sub> V <sub>LVW3H</sub> V <sub>LVW4H</sub>	Low-voltage warning thresholds — high range <ul style="list-style-type: none"> <li>• Level 1 falling (LVWV=00)</li> <li>• Level 2 falling (LVWV=01)</li> <li>• Level 3 falling (LVWV=10)</li> <li>• Level 4 falling (LVWV=11)</li> </ul>	2.62	2.70	2.78	V	1
		2.72	2.80	2.88	V	
		2.82	2.90	2.98	V	
		2.92	3.00	3.08	V	

Table continues on the next page...

**Table 2. V<sub>DD</sub> supply LVD and POR operating requirements (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>HYSH</sub>	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V <sub>LVDL</sub>	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V <sub>LVW1L</sub>	Low-voltage warning thresholds — low range					1
	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V <sub>LVW2L</sub>	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V <sub>LVW3L</sub>	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V <sub>LVW4L</sub>	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V <sub>HYSL</sub>	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V <sub>BG</sub>	Bandgap voltage reference	0.97	1.00	1.03	V	
t <sub>LPO</sub>	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

## 2.2.3 Voltage and current operating behaviors

**Table 3. Voltage and current operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>OH</sub>	Output high voltage — Normal drive pad except RESET_B					
	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OH</sub> = -5 mA	V <sub>DD</sub> - 0.5	—	—	V	1
	1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OH</sub> = -2.5 mA	V <sub>DD</sub> - 0.5	—	—	V	
V <sub>OH</sub>	Output high voltage — High drive pad except RESET_B					
	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OH</sub> = -20 mA	V <sub>DD</sub> - 0.5	—	—	V	1
	1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OH</sub> = -10 mA	V <sub>DD</sub> - 0.5	—	—	V	
I <sub>OHT</sub>	Output high current total for all ports	—	—	100	mA	
V <sub>OL</sub>	Output low voltage — Normal drive pad except RESET_B					
	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OL</sub> = 5 mA	—	—	0.5	V	1
	1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OL</sub> = 2.5 mA	—	—	0.5	V	
V <sub>OL</sub>	Output low voltage — High drive pad except RESET_B					
	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OL</sub> = 20 mA	—	—	0.5	V	1
	1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OL</sub> = 10 mA	—	—	0.5	V	
V <sub>OL</sub>	Output low voltage — RESET_B					

Table continues on the next page...



**Table 3. Voltage and current operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	2.7 V ≤ V <sub>DD</sub> ≤ 3.6 V, I <sub>OL</sub> = 3 mA	—	—	0.5	V	
	1.71 V ≤ V <sub>DD</sub> ≤ 2.7 V, I <sub>OL</sub> = 1.5 mA	—	—	0.5	V	
I <sub>OLT</sub>	Output low current total for all ports	—	—	100	mA	
I <sub>IN</sub>	Input leakage current (per pin) for full temperature range					
	All pins other than high drive port pins	—	0.002	0.5	μA	1, 2
	High drive port pins	—	0.004	0.5	μA	
I <sub>IN</sub>	Input leakage current (total all pins) for full temperature range	—	—	1.0	μA	2
R <sub>PU</sub>	Internal pullup resistors	20	—	50	kΩ	3
R <sub>PD</sub>	Internal pulldown resistors	20	—	50	kΩ	4

1. PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx\_PCRn[DSE] control bit. All other GPIOs are normal drive only.
2. Measured at V<sub>DD</sub>=3.6V
3. Measured at V<sub>DD</sub> supply voltage = V<sub>DD</sub> min and V<sub>input</sub> = V<sub>SS</sub>
4. Measured at V<sub>DD</sub> supply voltage = V<sub>DD</sub> min and V<sub>input</sub> = V<sub>DD</sub>

## 2.2.4 Power mode transition operating behaviors

All specifications except t<sub>POR</sub>, and VLLS<sub>x</sub>→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 80 MHz
- Bus clock = 40 MHz
- FlexBus clock = 20 MHz
- Flash clock = 20 MHz
- MCG mode: FEI

**Table 4. Power mode transition operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t <sub>POR</sub>	After a POR event, amount of time from the point V <sub>DD</sub> reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs	1
	• VLLS0 → RUN	—	—	140	μs	
	• VLLS1 → RUN	—	—	140	μs	

Table continues on the next page...

**Table 4. Power mode transition operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• VLLS2 → RUN	—	—	80	μs	
	• VLLS3 → RUN	—	—	80	μs	
	• LLS2 → RUN	—	—	6	μs	
	• LLS3 → RUN	—	—	6	μs	
	• VLPS → RUN	—	—	5.7	μs	
	• STOP → RUN	—	—	5.7	μs	

1. Normal boot (FTFA\_OPT[LPBOOT]=1)

## 2.2.5 Power consumption operating behaviors

The current parameters in the table below are derived from code executing a while(1) loop from flash, unless otherwise noted.

The IDD typical values represent the statistical mean at 25°C, and the IDD maximum values for RUN, WAIT, VLPR, and VLPW represent data collected at 125°C junction temperature unless otherwise noted. The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

**Table 5. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DDA</sub>	Analog supply current	—	—	See note	mA	1
I <sub>DD_HSRUN</sub>	High Speed Run mode current - all peripheral clocks disabled, CoreMark benchmark code executing from flash					
	@ 1.8V	—	28.0	29.33	mA	2, 3, 4
	@ 3.0V	—	28.0	29.33	mA	
I <sub>DD_HSRUN</sub>	High Speed Run mode current - all peripheral clocks disabled, code executing from flash					
	@ 1.8V	—	25.6	26.93	mA	2
	@ 3.0V	—	25.7	27.03	mA	
I <sub>DD_HSRUN</sub>	High Speed Run mode current — all peripheral clocks enabled, code executing from flash					

*Table continues on the next page...*

**Table 5. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	@ 1.8V @ 3.0V	— —	35.5 35.6	36.83 36.93	mA mA	5
I <sub>DD_RUN</sub>	Run mode current in Compute operation — CoreMark benchmark code executing from flash @ 1.8V @ 3.0V	— —	17.5 17.5	18.83 18.83	mA mA	3, 4, 6
I <sub>DD_RUN</sub>	Run mode current in Compute operation — code executing from flash @ 1.8V @ 3.0V	— —	15.10 15.10	17.10 17.33	mA mA	6
I <sub>DD_RUN</sub>	Run mode current — all peripheral clocks disabled, code executing from flash @ 1.8V @ 3.0V	— —	16.6 16.8	17.93 18.13	mA mA	7
I <sub>DD_RUN</sub>	Run mode current — all peripheral clocks enabled, code executing from flash @ 1.8V @ 3.0V • @ 25°C • @ 70°C • @ 85°C • @ 105°C	— — — — —	22.8 22.9 23.1 23.5 23.8	24.13 24.23 24.43 24.83 25.13	mA mA mA mA mA	8
I <sub>DD_RUN</sub>	Run mode current — Compute operation, code executing from flash @ 1.8V @ 3.0V • @ 25°C • @ 70°C • @ 85°C • @ 105°C	— — — — —	15.1 15.1 15.4 15.6 16.0	16.43 16.43 16.73 16.93 17.33	mA mA mA mA mA	9
I <sub>DD_WAIT</sub>	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	9.3	10.63	mA	7
I <sub>DD_WAIT</sub>	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.4	6.73	mA	10
I <sub>DD_VLPR</sub>	Very-low-power run mode current in Compute operation — CoreMark benchmark code executing from flash @ 1.8V @ 3.0V	— —	0.88 0.89	1.02 1.03	mA mA	3, 4, 11

Table continues on the next page...

**Table 5. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_VLPR</sub>	Very-low-power run mode current in Compute operation, code executing from flash @ 1.8V @ 3.0V	—	0.62	0.77	mA	11
		—	0.63	0.77	mA	
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.76	0.90	mA	12
I <sub>DD_VLPR</sub>	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	1.2	1.34	mA	13
I <sub>DD_VLPW</sub>	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.45	0.59	mA	14
I <sub>DD_STOP</sub>	Stop mode current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C @ 105°C	—	0.28	0.37	mA	
		—	0.34	0.51	mA	
		—	0.38	0.55	mA	
		—	0.50	0.80	mA	
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C @ 105°C	—	8.7	18.10	μA	
		—	31.1	79.55	μA	
		—	50.3	110.15	μA	
		—	98.6	238.30	μA	
I <sub>DD_LLS3</sub>	Low leakage stop mode 3 current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C @ 105°C	—	3.8	5.65	μA	
		—	12.5	28.75	μA	
		—	20.2	47.60	μA	
		—	39.5	91.25	μA	
I <sub>DD_LLS2</sub>	Low leakage stop mode 2 current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C @ 105°C	—	3.0	4.10	μA	
		—	7.8	16.40	μA	
		—	12.3	30.15	μA	
		—	23.6	55.30	μA	
I <sub>DD_VLLS3</sub>	Very low-leakage stop mode 3 current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C @ 105°C	—	2.8	3.95	μA	
		—	9.5	21.25	μA	
		—	15.3	34.65	μA	
		—	30.1	66.05	μA	
I <sub>DD_VLLS2</sub>	Very low-leakage stop mode 2 current at 3.0 V @ -40°C to 25°C @ 70°C @ 85°C @ 105°C	—	1.9	2.45	μA	
		—	4.5	8.50	μA	
		—	6.8	12.15	μA	
		—	13.0	25.50	μA	

Table continues on the next page...

**Table 5. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_VLLS1</sub>	Very low-leakage stop mode 1 current at 3.0 V @ -40°C to 25°C	—	0.73	1.42	μA	
	@ 70°C	—	1.8	3.90	μA	
	@ 85°C	—	3.0	5.25	μA	
	@ 105°C	—	5.9	10.80	μA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled	—	0.43	0.55	μA	
	@ -40°C to 25°C	—	1.4	2.45	μA	
	@ 70°C	—	2.6	4.00	μA	
	@ 85°C	—	5.4	9.30	μA	
I <sub>DD_VLLS0</sub>	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled	—	0.14	0.24	μA	
	@ -40°C to 25°C	—	1.1	2.15	μA	
	@ 70°C	—	2.3	3.85	μA	
	@ 85°C	—	5.1	9.00	μA	

- The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
- 120MHz core and system clock, 60MHz bus clock, 24MHz FlexBus clock, and 24MHz flash clock. MCG configured for PEE mode. All peripheral clocks disabled.
- Cache on and prefetch on, low compiler optimization.
- Coremark benchmark compiled using IAR 7.2 with optimization level low.
- 120MHz core and system clock, 60MHz bus clock, 24MHz FlexBus clock, and 24MHz flash clock. MCG configured for PEE mode. All peripheral clocks enabled.
- 80 MHz core and system clock, 40 MHz bus clock, and 26.67 MHz flash clock. MCG configured for PEE mode. Compute operation.
- 80MHz core and system clock, 40MHz bus clock, 20MHz FlexBus clock, and 26.67MHz flash clock. MCG configured for FEI mode. All peripheral clocks disabled.
- 80MHz core and system clock, 40MHz bus clock, 20MHz FlexBus clock, and 26.67MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled.
- 80MHz core and system clock, 40MHz bus clock, and 26.67MHz flash clock. MCG configured for FEI mode. Compute operation.
- 25MHz core and system clock, 25MHz bus clock, and 25MHz FlexBus and flash clock. MCG configured for FEI mode.
- 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. Compute operation. Code executing from flash.
- 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
- 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
- 4 MHz core, system, FlexBus, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.

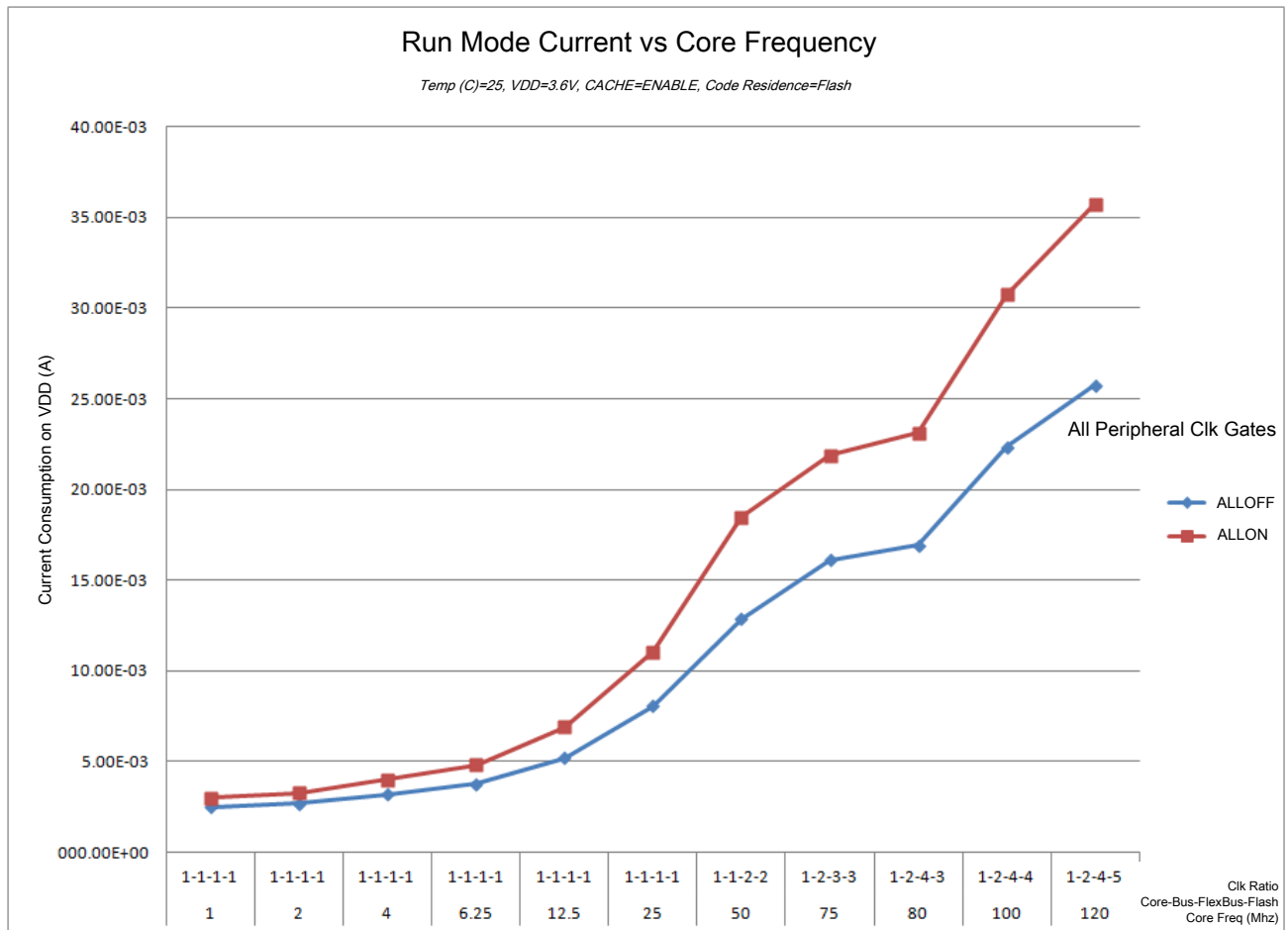
**Table 6. Low power mode peripheral adders—typical value**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I <sub>IREFSTEN4MHz</sub>	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA
I <sub>IREFSTEN32KHz</sub>	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	μA
I <sub>EREFSTEN4MHz</sub>	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
I <sub>EREFSTEN32KHz</sub>	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							
	VLLS1	440	490	540	560	570	580	nA
	VLLS3	440	490	540	560	570	580	
	LLS	490	490	540	560	570	680	
	VLPS	510	560	560	560	610	680	
	STOP	510	560	560	560	610	680	
I <sub>48MIRC</sub>	48 Mhz internal reference clock	350	350	350	350	350	350	μA
I <sub>CMP</sub>	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I <sub>UART</sub>	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	μA
	>OSCERCLK (4 MHz external crystal)	214	237	246	254	260	268	
I <sub>BG</sub>	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	μA
I <sub>ADC</sub>	ADC peripheral adder combining the measured values at V <sub>DD</sub> and V <sub>DDA</sub> by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	42	42	42	42	42	42	μA

### 2.2.5.1 Diagram: Typical IDD\_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode for 50 MHz and lower frequencies. MCG in FEE mode at frequencies between 50 MHz and 100MHz. MCG in PEE mode at frequencies greater than 100 MHz.
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA



**Figure 3. Run mode supply current vs. core frequency**

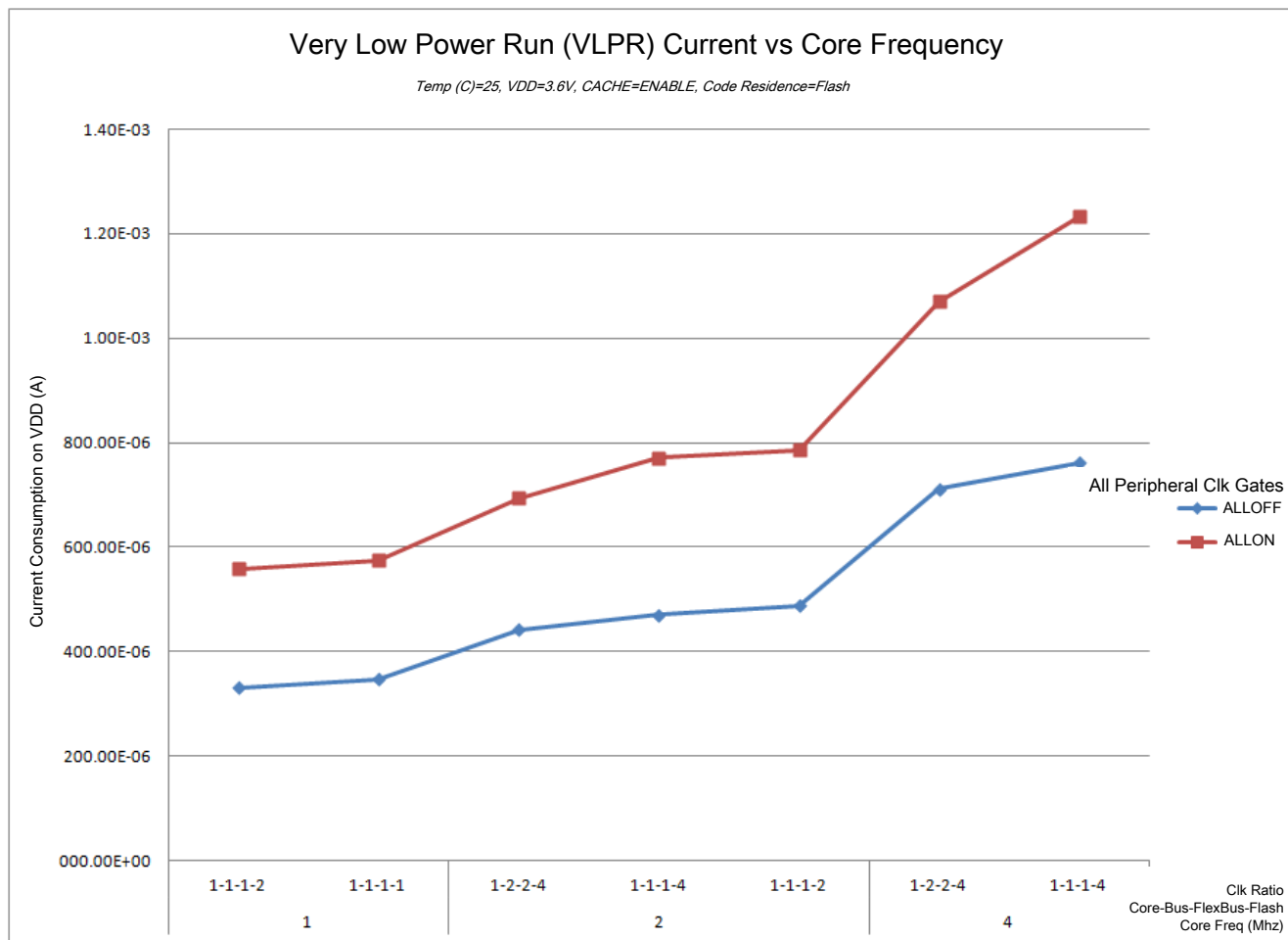


Figure 4. VLPR mode supply current vs. core frequency

## 2.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors for 64 LQFP package

Parameter	Conditions	Clocks	Frequency range	Level (Typ.)	Unit	Notes
V <sub>EME</sub>	Device configuration, test conditions and EM testing per standard IEC 61967-2. Supply voltages: • VDD = 3.3 V Temp = 25°C	FSYS = 120 MHz FBUS = 60 MHz External crystal = 8 MHz	150 kHz–50 MHz	14	dBuV	1, 2, 3
			50 MHz–150 MHz	23		
			150 MHz–500 MHz	23		
			500 MHz–1000 MHz	9		
			IEC level	L		4

1. Measurements were made per IEC 61967-2 while the device was running typical application code.
2. Measurements were performed on a similar 64LQFP device.
3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.



4. IEC Level Maximums: M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV, H ≤ 42dBmV .

## 2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to [www.freescale.com](http://www.freescale.com).
2. Perform a keyword search for “EMC design.”

## 2.2.8 Capacitance attributes

**Table 8. Capacitance attributes**

Symbol	Description	Min.	Max.	Unit
C <sub>IN_A</sub>	Input capacitance: analog pins	—	7	pF
C <sub>IN_D</sub>	Input capacitance: digital pins	—	7	pF

## 2.3 Switching specifications

### 2.3.1 Device clock specifications

**Table 9. Device clock specifications**

Symbol	Description	Min.	Max.	Unit	Notes
High Speed run mode					
f <sub>SYS</sub>	System and core clock	—	120	MHz	
f <sub>BUS</sub>	Bus clock	—	60	MHz	
Normal run mode (and High Speed run mode unless otherwise specified above)					
f <sub>SYS</sub>	System and core clock	—	80	MHz	
f <sub>BUS</sub>	Bus clock	—	50	MHz	
FB_CLK	FlexBus clock	—	30	MHz	
f <sub>FLASH</sub>	Flash clock	—	26.67	MHz	
f <sub>LPTMR</sub>	LPTMR clock	—	25	MHz	
VLPR mode <sup>1</sup>					
f <sub>SYS</sub>	System and core clock	—	4	MHz	
f <sub>BUS</sub>	Bus clock	—	4	MHz	
FB_CLK	FlexBus clock	—	4	MHz	

*Table continues on the next page...*

**Table 9. Device clock specifications (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
f <sub>FLASH</sub>	Flash clock	—	1	MHz	
f <sub>ERCLK</sub>	External reference clock	—	16	MHz	
f <sub>LPTMR_pin</sub>	LPTMR clock	—	25	MHz	
f <sub>LPTMR_ERCLK</sub>	LPTMR external reference clock	—	16	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

### 2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

**Table 10. General switching specifications**

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	4
	Mode select (EZP_CS) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time				5
	<ul style="list-style-type: none"> <li>• Slew disabled <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> <li>• Slew enabled <ul style="list-style-type: none"> <li>• <math>1.71 \leq V_{DD} \leq 2.7V</math></li> <li>• <math>2.7 \leq V_{DD} \leq 3.6V</math></li> </ul> </li> </ul>	—	—		
		—	10	ns	
		—	5	ns	
		—	30	ns	
		—	16	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
5. 25 pF load

## 2.4 Thermal specifications

### 2.4.1 Thermal operating requirements

**Table 11. Thermal operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
T <sub>J</sub>	Die junction temperature	-40	125	°C	
T <sub>A</sub>	Ambient temperature	-40	105	°C	1

1. Maximum T<sub>A</sub> can be exceeded only if the user ensures that T<sub>J</sub> does not exceed maximum T<sub>J</sub>. The simplest method to determine T<sub>J</sub> is: T<sub>J</sub> = T<sub>A</sub> + R<sub>θJA</sub> × chip power dissipation.

### 2.4.2 Thermal attributes

Board type	Symbol	Description	100 LQFP	64 LQFP	Unit	Notes
Single-layer (1s)	R <sub>θJA</sub>	Thermal resistance, junction to ambient (natural convection)	61	67	°C/W	1
Four-layer (2s2p)	R <sub>θJA</sub>	Thermal resistance, junction to ambient (natural convection)	48	48	°C/W	2
Single-layer (1s)	R <sub>θJMA</sub>	Thermal resistance, junction to ambient (200 ft./min. air speed)	51	55	°C/W	3
Four-layer (2s2p)	R <sub>θJMA</sub>	Thermal resistance, junction to ambient (200 ft./min. air speed)	42	42	°C/W	3
—	R <sub>θJB</sub>	Thermal resistance, junction to board	34	31	°C/W	4
—	R <sub>θJC</sub>	Thermal resistance, junction to case	16	16	°C/W	5
—	Ψ <sub>JT</sub>	Thermal characterization parameter, junction to package top outside center (natural convection)	3	3	°C/W	6

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. Board meets JESD51-9 specification.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
4. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

### 3 Peripheral operating requirements and behaviors

#### 3.1 Core modules

##### 3.1.1 SWD electricals

Table 12. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	SWD_CLK frequency of operation <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul>	0	33	MHz
S2	SWD_CLK cycle period	1/S1	—	ns
S3	SWD_CLK clock pulse width <ul style="list-style-type: none"> <li>Serial wire debug</li> </ul>	15	—	ns
S4	SWD_CLK rise and fall times	—	3	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	8	—	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	1.4	—	ns
S11	SWD_CLK high to SWD_DIO data valid	—	25	ns
S12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

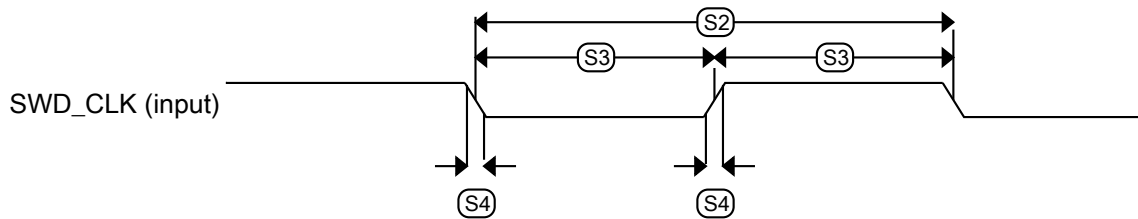


Figure 5. Serial wire clock input timing

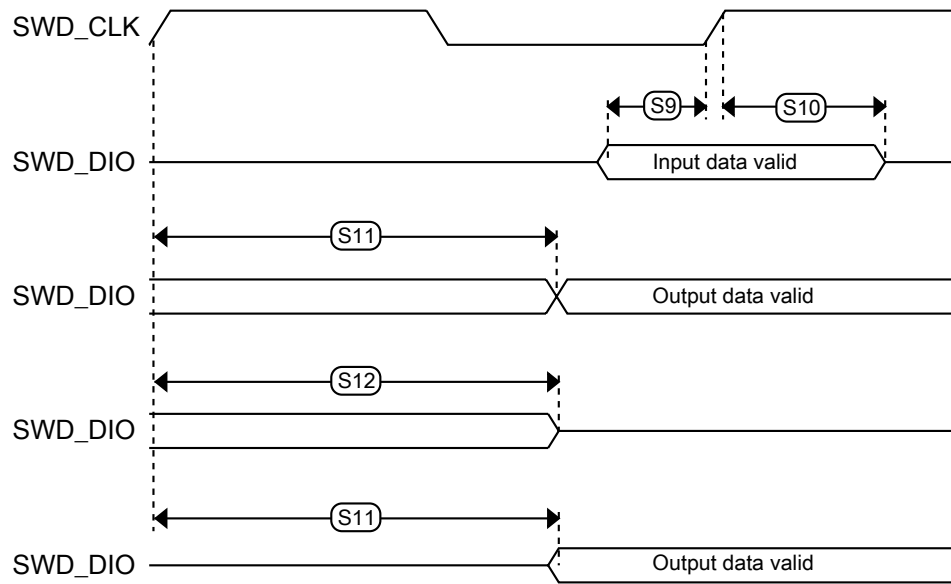


Figure 6. Serial wire data timing

### 3.1.2 JTAG electricals

Table 13. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns

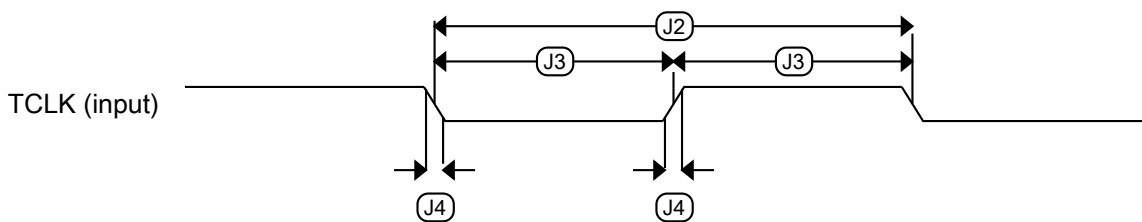
Table continues on the next page...

**Table 13. JTAG limited voltage range electricals (continued)**

Symbol	Description	Min.	Max.	Unit
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

**Table 14. JTAG full voltage range electricals**

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> </ul>	0 0	10 15	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width <ul style="list-style-type: none"> <li>• Boundary Scan</li> <li>• JTAG and CJTAG</li> </ul>	50 33	— —	ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.4	—	ns
J7	TCLK low to boundary scan output data valid	—	27	ns
J8	TCLK low to boundary scan output high-Z	—	27	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	26.2	ns
J12	TCLK low to TDO high-Z	—	26.2	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns



**Figure 7. Test clock input timing**

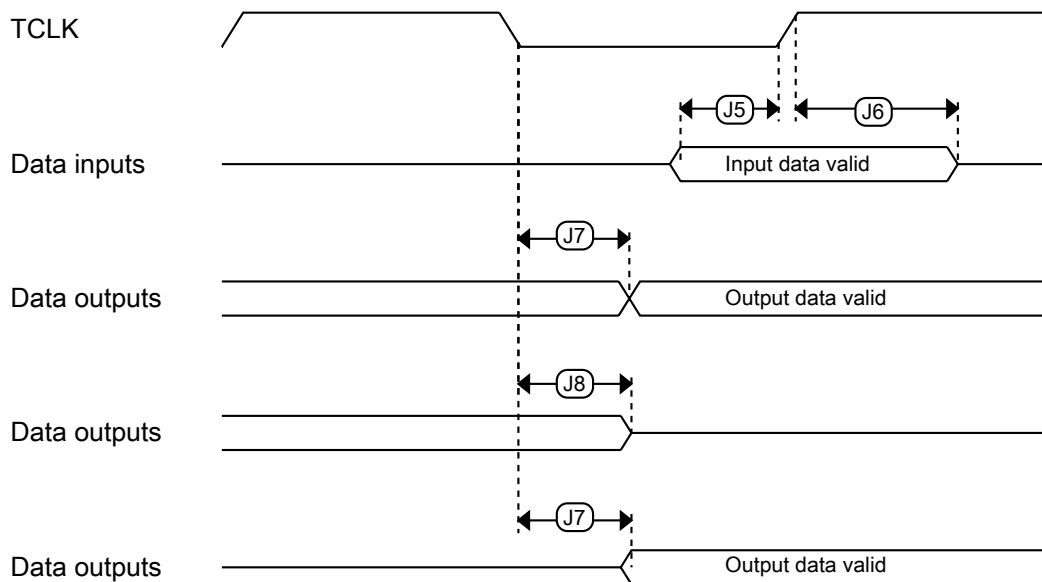


Figure 8. Boundary scan (JTAG) timing

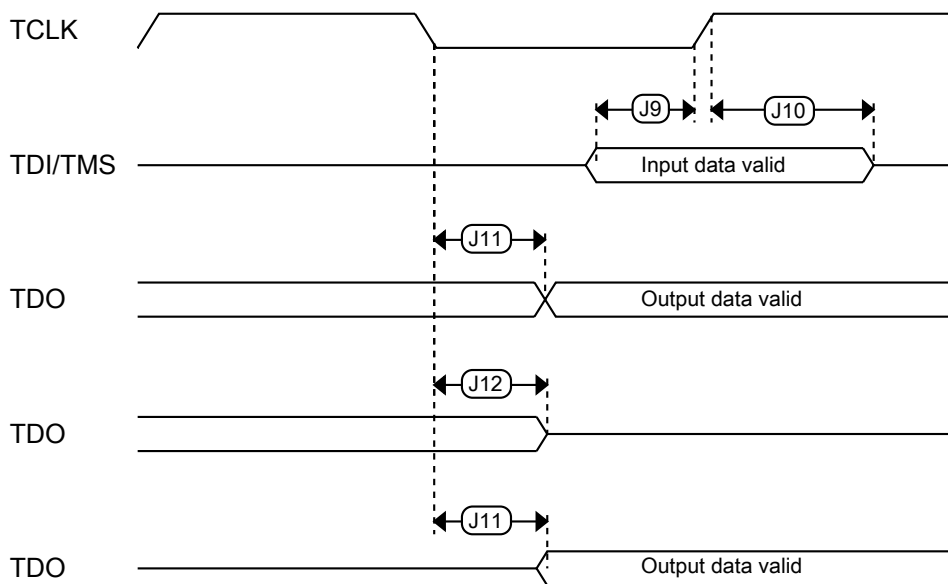


Figure 9. Test Access Port timing

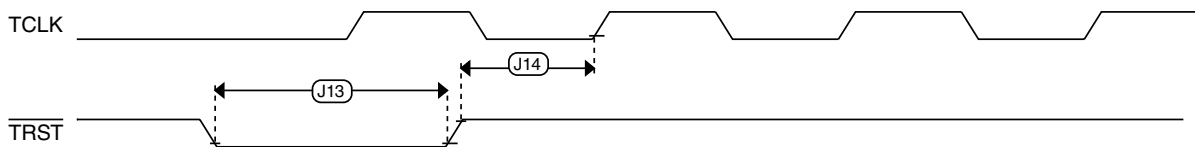


Figure 10. TRST timing

## 3.2 System modules

There are no specifications necessary for the device's system modules.

## 3.3 Clock modules

### 3.3.1 MCG specifications

Table 15. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{ints\_ft}$	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
$\Delta f_{ints\_t}$	Total deviation of internal reference frequency (slow clock) over voltage and temperature	—	+0.5/-0.7	± 2	%	
$f_{ints\_t}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	% $f_{dco}$	1
$\Delta f_{dco\_t}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+0.5/-0.7	± 2	% $f_{dco}$	1, 2
$\Delta f_{dco\_t}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.3	± 1.5	% $f_{dco}$	1
$f_{intf\_ft}$	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
$\Delta f_{intf\_ft}$	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal VDD and 25 °C	—	+1/-2	± 5	% $f_{intf\_ft}$	
$f_{intf\_t}$	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	

Table continues on the next page...



**Table 15. MCG specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
$f_{loc\_low}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{ints\_t}$	—	—	kHz		
$f_{loc\_high}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{ints\_t}$	—	—	kHz		
FLL							
$f_{fill\_ref}$	FLL reference frequency range	31.25	—	39.0625	kHz		
$f_{dco}$	DCO output frequency range	Low range (DRS=00) $640 \times f_{fill\_ref}$	20	20.97	25	MHz	3, 4
		Mid range (DRS=01) $1280 \times f_{fill\_ref}$	40	41.94	50	MHz	
		Mid-high range (DRS=10) $1920 \times f_{fill\_ref}$	60	62.91	75	MHz	
		High range (DRS=11) $2560 \times f_{fill\_ref}$	80	83.89	100	MHz	
$f_{dco\_t\_DMX3}$ 2	DCO output frequency	Low range (DRS=00) $732 \times f_{fill\_ref}$	—	23.99	—	MHz	5, 6
		Mid range (DRS=01) $1464 \times f_{fill\_ref}$	—	47.97	—	MHz	
		Mid-high range (DRS=10) $2197 \times f_{fill\_ref}$	—	71.99	—	MHz	
		High range (DRS=11) $2929 \times f_{fill\_ref}$	—	95.98	—	MHz	
$J_{cyc\_fill}$	FLL period jitter <ul style="list-style-type: none"> <li><math>f_{VCO} = 48</math> MHz</li> <li><math>f_{VCO} = 98</math> MHz</li> </ul>	—	— 180 150	—	ps		
$t_{fill\_acquire}$	FLL target frequency acquisition time	—	—	1	ms	7	
PLL							
$f_{vco}$	VCO operating frequency	48.0	—	120	MHz		
$I_{pll}$	PLL operating current <ul style="list-style-type: none"> <li>PLL @ 96 MHz (<math>f_{osc\_hi\_1} = 8</math> MHz, <math>f_{pll\_ref} = 2</math> MHz, VDIV multiplier = 48)</li> </ul>	—	1060	—	$\mu$ A	8	
$I_{pll}$	PLL operating current <ul style="list-style-type: none"> <li>PLL @ 48 MHz (<math>f_{osc\_hi\_1} = 8</math> MHz, <math>f_{pll\_ref} = 2</math> MHz, VDIV multiplier = 24)</li> </ul>	—	600	—	$\mu$ A	8	
$f_{pll\_ref}$	PLL reference frequency range	2.0	—	4.0	MHz		
$J_{cyc\_pll}$	PLL period jitter (RMS) <ul style="list-style-type: none"> <li><math>f_{vco} = 48</math> MHz</li> <li><math>f_{vco} = 100</math> MHz</li> </ul>	—	120	—	ps	9	
		—	75	—	ps		
$J_{acc\_pll}$	PLL accumulated jitter over 1 $\mu$ s (RMS)					9	

Table continues on the next page...

**Table 15. MCG specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	<ul style="list-style-type: none"> <li><math>f_{VCO} = 48 \text{ MHz}</math></li> <li><math>f_{VCO} = 100 \text{ MHz}</math></li> </ul>	—	1350	—	ps	
		—	600	—	ps	
$D_{lock}$	Lock entry frequency tolerance	$\pm 1.49$	—	$\pm 2.98$	%	
$D_{unl}$	Lock exit frequency tolerance	$\pm 4.47$	—	$\pm 5.97$	%	
$t_{pll\_lock}$	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	10

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2.  $2.0 \text{ V} \leq VDD \leq 3.6 \text{ V}$ .
3. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
4. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation ( $\Delta f_{dco\_t}$ ) over voltage and temperature should be considered.
5. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
6. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
7. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
8. Excludes any oscillator currents that are also consuming power while PLL is in operation.
9. This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
10. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

### 3.3.2 IRC48M specifications

**Table 16. IRC48M specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	—	3.6	V	
$I_{DD48M}$	Supply current	—	400	500	$\mu\text{A}$	
$f_{irc48m}$	Internal reference frequency	—	48	—	MHz	
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage ( $VDD=1.89\text{V}-3.6\text{V}$ ) over $0^\circ\text{C}$ to $70^\circ\text{C}$	—	$\pm 0.2$	$\pm 0.5$	$\%f_{irc48m}$	1
$\Delta f_{irc48m\_ol\_hv}$	Open loop total deviation of IRC48M frequency at high voltage ( $VDD=1.89\text{V}-3.6\text{V}$ ) over full temperature	—	$\pm 0.4$	$\pm 1.0$	$\%f_{irc48m}$	1
$\Delta f_{irc48m\_ol\_lv}$	Open loop total deviation of IRC48M frequency at low voltage ( $VDD=1.71\text{V}-1.89\text{V}$ ) over full temperature	—	$\pm 0.5$	$\pm 1.5$	$\%f_{irc48m}$	1
$J_{cyc\_irc48m}$	Period Jitter (RMS)	—	35	150	ps	
$t_{irc48mst}$	Startup time	—	2	3	$\mu\text{s}$	2

1. The maximum value represents characterized results equivalent to the mean plus or minus three times the standard deviation (mean  $\pm 3$  sigma).

2. IRC48M startup time is defined as the time between clock enablement and clock availability for system use. Enable the clock by one of the following settings:
- MCG operating in an external clocking mode and MCG\_C7[OSCSEL]=10 or MCG\_C5[PLLCLKEN0]=1, or
  - SIM\_SOPT2[PLLFLSEL]=11

### 3.3.3 Oscillator electrical specifications

#### 3.3.3.1 Oscillator DC electrical specifications

Table 17. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>DD</sub>	Supply voltage	1.71	—	3.6	V	
I <sub>DDOSC</sub>	Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 4 MHz</li> <li>• 8 MHz (RANGE=01)</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	500	—	nA	1
I <sub>DDOSC</sub>	Supply current — high-gain mode (HGO=1) <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 4 MHz</li> <li>• 8 MHz (RANGE=01)</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	25	—	μA	1
C <sub>x</sub>	EXTAL load capacitance	—	—	—		2, 3
C <sub>y</sub>	XTAL load capacitance	—	—	—		2, 3
R <sub>F</sub>	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R <sub>S</sub>	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	

Table continues on the next page...

**Table 17. Oscillator DC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V <sub>pp</sub> <sup>5</sup>	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V <sub>DD</sub>	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V <sub>DD</sub>	—	V	

1. V<sub>DD</sub>=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C<sub>x</sub> and C<sub>y</sub> can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R<sub>F</sub> is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

### 3.3.3.2 Oscillator frequency specifications

**Table 18. Oscillator frequency specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f <sub>osc_lo</sub>	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
f <sub>osc_hi_1</sub>	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
f <sub>osc_hi_2</sub>	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f <sub>ec_extal</sub>	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t <sub>dc_extal</sub>	Input clock duty cycle (external clock mode)	40	50	60	%	
t <sub>cst</sub>	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	

Table continues on the next page...

**Table 18. Oscillator frequency specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG\_S register being set.

## 3.4 Memories and memory interfaces

### 3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

#### 3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 19. NVM program/erase timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvpgm4}$	Longword Program high-voltage time	—	7.5	18	$\mu$ s	—
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversblk256k}$	Erase Block high-voltage time for 256 KB	—	104	904	ms	1

1. Maximum time based on expectations at cycling end-of-life.

#### 3.4.1.2 Flash timing specifications — commands

**Table 20. Flash command timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					1

*Table continues on the next page...*

**Table 20. Flash command timing specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk256k}$	• 256 KB program flash	—	—	1.7	ms	
$t_{rd1sec2k}$	Read 1s Section execution time (flash sector)	—	—	60	$\mu$ s	1
$t_{pgmchk}$	Program Check execution time	—	—	45	$\mu$ s	1
$t_{rdsrc}$	Read Resource execution time	—	—	30	$\mu$ s	1
$t_{pgm4}$	Program Longword execution time	—	65	145	$\mu$ s	—
$t_{ersblk256k}$	Erase Flash Block execution time • 256 KB program flash	—	250	1500	ms	2
$t_{ersscr}$	Erase Flash Sector execution time	—	14	114	ms	2
$t_{rd1all}$	Read 1s All Blocks execution time	—	—	1.8	ms	1
$t_{rdonce}$	Read Once execution time	—	—	30	$\mu$ s	1
$t_{pgmonce}$	Program Once execution time	—	100	—	$\mu$ s	—
$t_{ersall}$	Erase All Blocks execution time	—	500	3000	ms	2
$t_{vfykey}$	Verify Backdoor Access Key execution time	—	—	30	$\mu$ s	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

### 3.4.1.3 Flash high voltage current behaviors

**Table 21. Flash high voltage current behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{DD\_PGM}$	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
$I_{DD\_ERS}$	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

### 3.4.1.4 Reliability specifications

**Table 22. NVM reliability specifications**

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at  $-40\text{ °C} \leq T_j \leq 125\text{ °C}$ .

### 3.4.2 EzPort switching specifications

Table 23. EzPort switching specifications

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
EP1	EZP_CK frequency of operation (all commands except READ)	—	$f_{SYS}/2$	MHz
EP1a	EZP_CK frequency of operation (READ command)	—	$f_{SYS}/8$	MHz
EP2	$\overline{\text{EZP\_CS}}$ negation to next $\overline{\text{EZP\_CS}}$ assertion	$2 \times t_{\text{EZP\_CK}}$	—	ns
EP3	$\overline{\text{EZP\_CS}}$ input valid to EZP_CK high (setup)	5	—	ns
EP4	EZP_CK high to $\overline{\text{EZP\_CS}}$ input invalid (hold)	5	—	ns
EP5	EZP_D input valid to EZP_CK high (setup)	2	—	ns
EP6	EZP_CK high to EZP_D input invalid (hold)	5	—	ns
EP7	EZP_CK low to EZP_Q output valid	—	25	ns
EP8	EZP_CK low to EZP_Q output invalid (hold)	0	—	ns
EP9	$\overline{\text{EZP\_CS}}$ negation to EZP_Q tri-state	—	12	ns

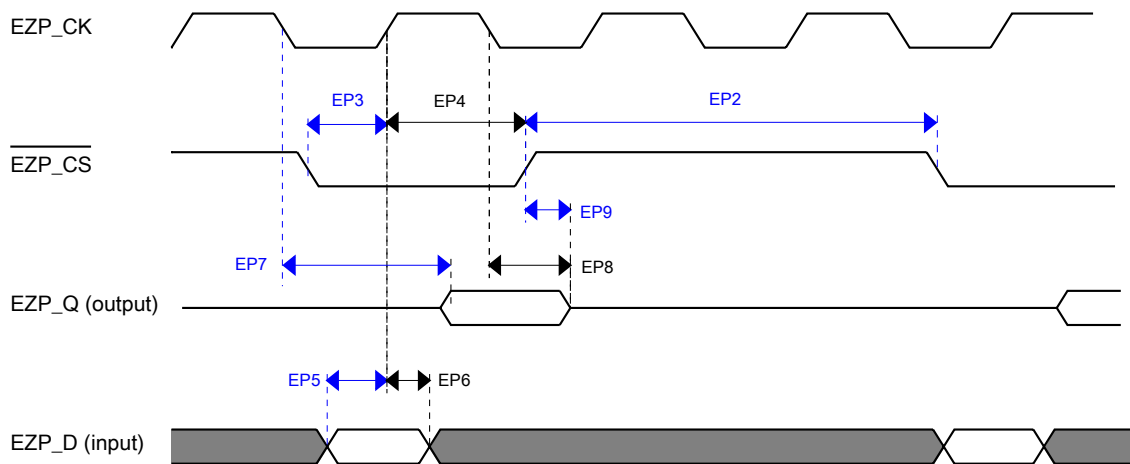


Figure 11. EzPort Timing Diagram

### 3.4.3 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB\_CLK. The FB\_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB\_CLK). All other timing relationships can be derived from these values.

**Table 24. Flexbus limited voltage range switching specifications**

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
FB1	Clock period	33.3	—	ns	
FB2	Address, data, and control output valid	—	15	ns	
FB3	Address, data, and control output hold	0.5	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	14.5	—	ns	
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB\_AD[31:0],  $\overline{\text{FB\_BE/BWEn}}$ ,  $\overline{\text{FB\_CSn}}$ ,  $\overline{\text{FB\_OE}}$ , FB\_R/W, FB\_TBST, FB\_TSIZ[1:0], FB\_ALE, and FB\_TS.
2. Specification is valid for all FB\_AD[31:0] and  $\overline{\text{FB\_TA}}$ .

**Table 25. Flexbus full voltage range switching specifications**

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	
	Frequency of operation	—	30	MHz	
FB1	Clock period	33.3	—	ns	
FB2	Address, data, and control output valid	—	21.5	ns	
FB3	Address, data, and control output hold	-1.0	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	20.0	—	ns	
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	0.5	—	ns	2

1. Specification is valid for all FB\_AD[31:0],  $\overline{\text{FB\_BE/BWEn}}$ ,  $\overline{\text{FB\_CSn}}$ ,  $\overline{\text{FB\_OE}}$ , FB\_R/W, FB\_TBST, FB\_TSIZ[1:0], FB\_ALE, and FB\_TS.
2. Specification is valid for all FB\_AD[31:0] and  $\overline{\text{FB\_TA}}$ .



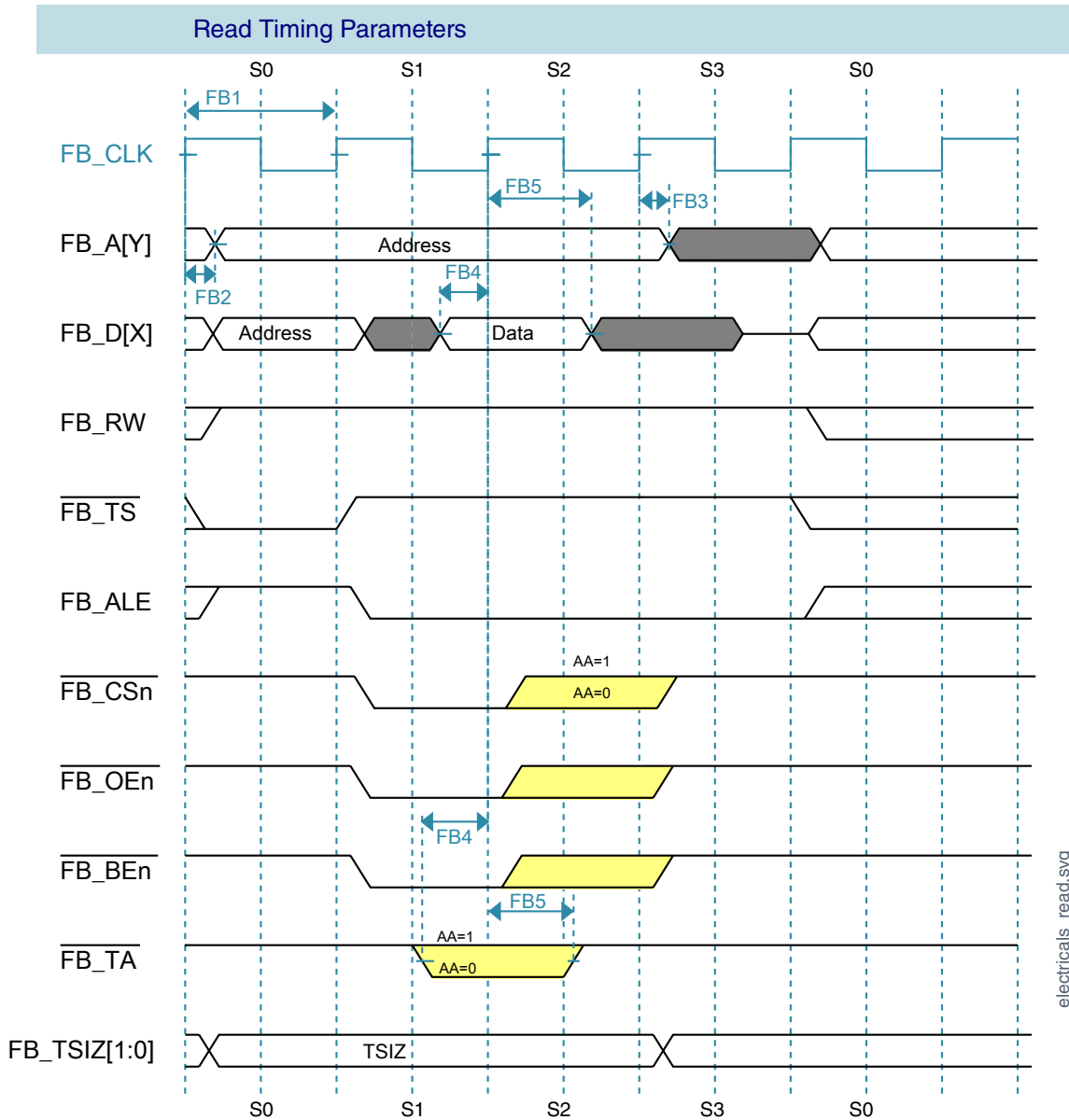


Figure 12. FlexBus read timing diagram

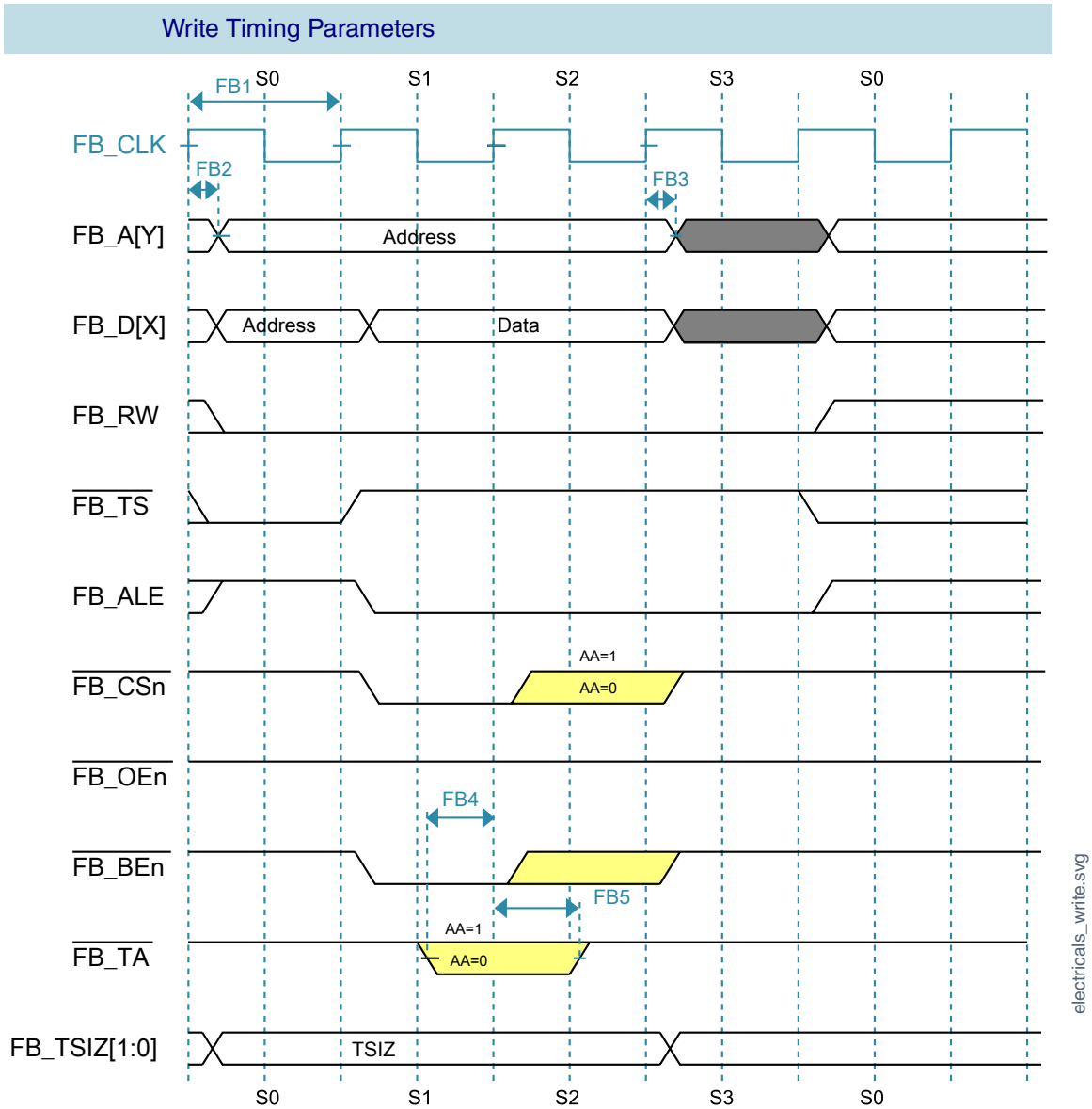


Figure 13. FlexBus write timing diagram

electricals\_write.svg

### 3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

### 3.6 Analog

### 3.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 26](#) and [Table 27](#) are achievable on the differential pins ADCx\_DPx, ADCx\_DMx.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

#### 3.6.1.1 16-bit ADC operating conditions

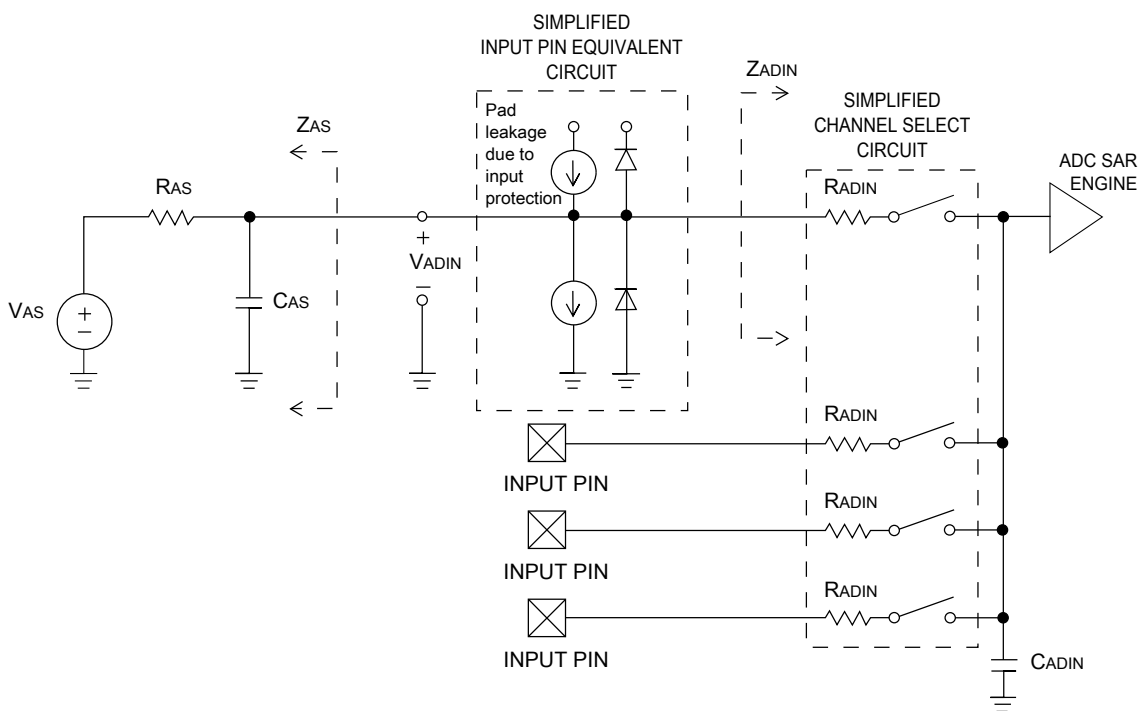
**Table 26. 16-bit ADC operating conditions**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	Absolute	1.71	—	3.6	V	
ΔV <sub>DDA</sub>	Supply voltage	Delta to V <sub>DD</sub> (V <sub>DD</sub> – V <sub>DDA</sub> )	-100	0	+100	mV	2
ΔV <sub>SSA</sub>	Ground voltage	Delta to V <sub>SS</sub> (V <sub>SS</sub> – V <sub>SSA</sub> )	-100	0	+100	mV	2
V <sub>REFH</sub>	ADC reference voltage high		1.13	V <sub>DDA</sub>	V <sub>DDA</sub>	V	
V <sub>REFL</sub>	ADC reference voltage low		V <sub>SSA</sub>	V <sub>SSA</sub>	V <sub>SSA</sub>	V	
V <sub>ADIN</sub>	Input voltage	<ul style="list-style-type: none"> <li>16-bit differential mode</li> <li>All other modes</li> </ul>	V <sub>REFL</sub> V <sub>REFL</sub>	— —	31/32 * V <sub>REFH</sub> V <sub>REFH</sub>	V	
C <sub>ADIN</sub>	Input capacitance	<ul style="list-style-type: none"> <li>16-bit mode</li> <li>8-bit / 10-bit / 12-bit modes</li> </ul>	— —	8 4	10 5	pF	
R <sub>ADIN</sub>	Input series resistance		—	2	5	kΩ	
R <sub>AS</sub>	Analog source resistance (external)	13-bit / 12-bit modes f <sub>ADCK</sub> < 4 MHz	—	—	5	kΩ	3
f <sub>ADCK</sub>	ADC conversion clock frequency	≤ 13-bit mode	1.0	—	24.0	MHz	4
f <sub>ADCK</sub>	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	4
C <sub>rate</sub>	ADC conversion rate	≤ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20	—	1200	Ksps	5
C <sub>rate</sub>	ADC conversion rate	16-bit mode No ADC hardware averaging	37	—	461	Ksps	5

**Table 26. 16-bit ADC operating conditions**

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
		Continuous conversions enabled, subsequent conversion time					

1. Typical values assume  $V_{DDA} = 3.0\text{ V}$ ,  $\text{Temp} = 25\text{ }^\circ\text{C}$ ,  $f_{ADCK} = 1.0\text{ MHz}$ , unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had  $< 8\ \Omega$  analog source resistance. The  $R_{AS}/C_{AS}$  time constant should be kept to  $< 1\text{ ns}$ .
4. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
5. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).



**Figure 14. ADC input impedance equivalency diagram**

### 3.6.1.2 16-bit ADC electrical characteristics

**Table 27. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )**

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$I_{DDA\_ADC}$	Supply current		0.215	—	1.7	mA	3

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**Table 27. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

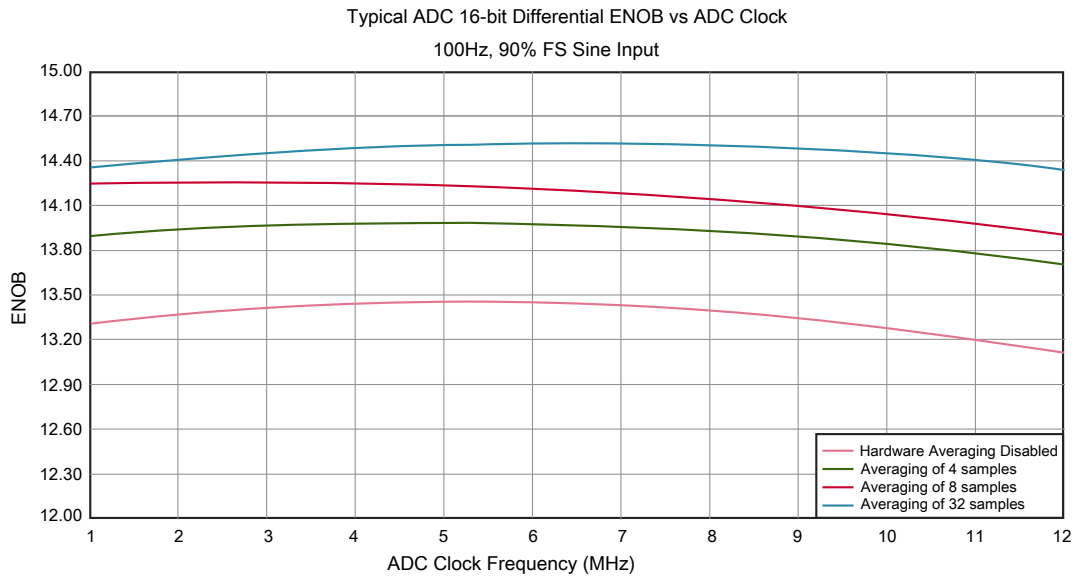
Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$f_{ADACK}$	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/f_{ADACK}$
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	—	±4	±6.8	LSB <sup>4</sup>	5
DNL	Differential non-linearity	• 12-bit modes	—	±0.7	-1.1 to +1.9	LSB <sup>4</sup>	5
		• <12-bit modes	—	±0.2	-0.3 to 0.5		
INL	Integral non-linearity	• 12-bit modes	—	±1.0	-2.7 to +1.9	LSB <sup>4</sup>	5
		• <12-bit modes	—	±0.5	-0.7 to +0.5		
$E_{FS}$	Full-scale error	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	—	-4	-5.4	LSB <sup>4</sup>	$V_{ADIN} = V_{DDA}$ <sup>5</sup>
$E_Q$	Quantization error	• 16-bit modes	—	-1 to 0	—	LSB <sup>4</sup>	
		• ≤13-bit modes	—	—	±0.5		
ENOB	Effective number of bits	16-bit differential mode					6
		• Avg = 32	12.8	14.5	—	bits	
		• Avg = 4	11.9	13.8	—	bits	
		16-bit single-ended mode					
• Avg = 32	12.2	13.9	—	bits			
• Avg = 4	11.4	13.1	—	bits			
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode				dB	7
		• Avg = 32	—	-94	—	dB	
		16-bit single-ended mode					
		• Avg = 32	—	-85	—		
SFDR	Spurious free dynamic range	16-bit differential mode				dB	7
		• Avg = 32	82	95	—	dB	
		16-bit single-ended mode	78	90	—		

Table continues on the next page...

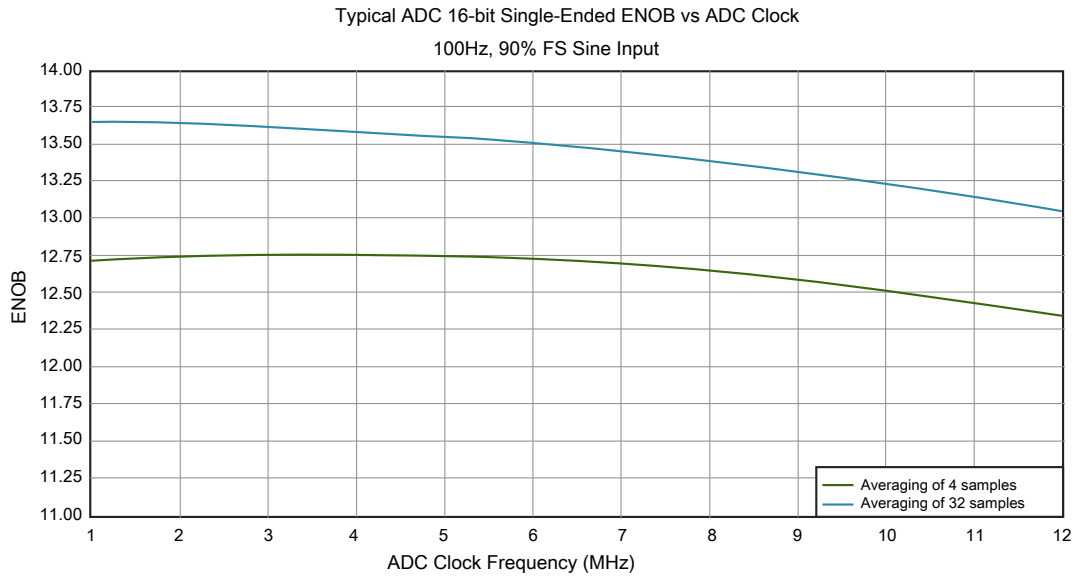
**Table 27. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
		• Avg = 32					
$E_{IL}$	Input leakage error		$I_{in} \times R_{AS}$			mV	$I_{in}$ = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
$V_{TEMP25}$	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with  $V_{REFH} = V_{DDA}$
2. Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25 °C,  $f_{ADCK} = 2.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC\_CFG1[ADLPC] (low power). For lowest power operation, ADC\_CFG1[ADLPC] must be set, the ADC\_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4.  $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz



**Figure 15. Typical ENOB vs. ADC\_CLK for 16-bit differential mode**



**Figure 16. Typical ENOB vs. ADC\_CLK for 16-bit single-ended mode**

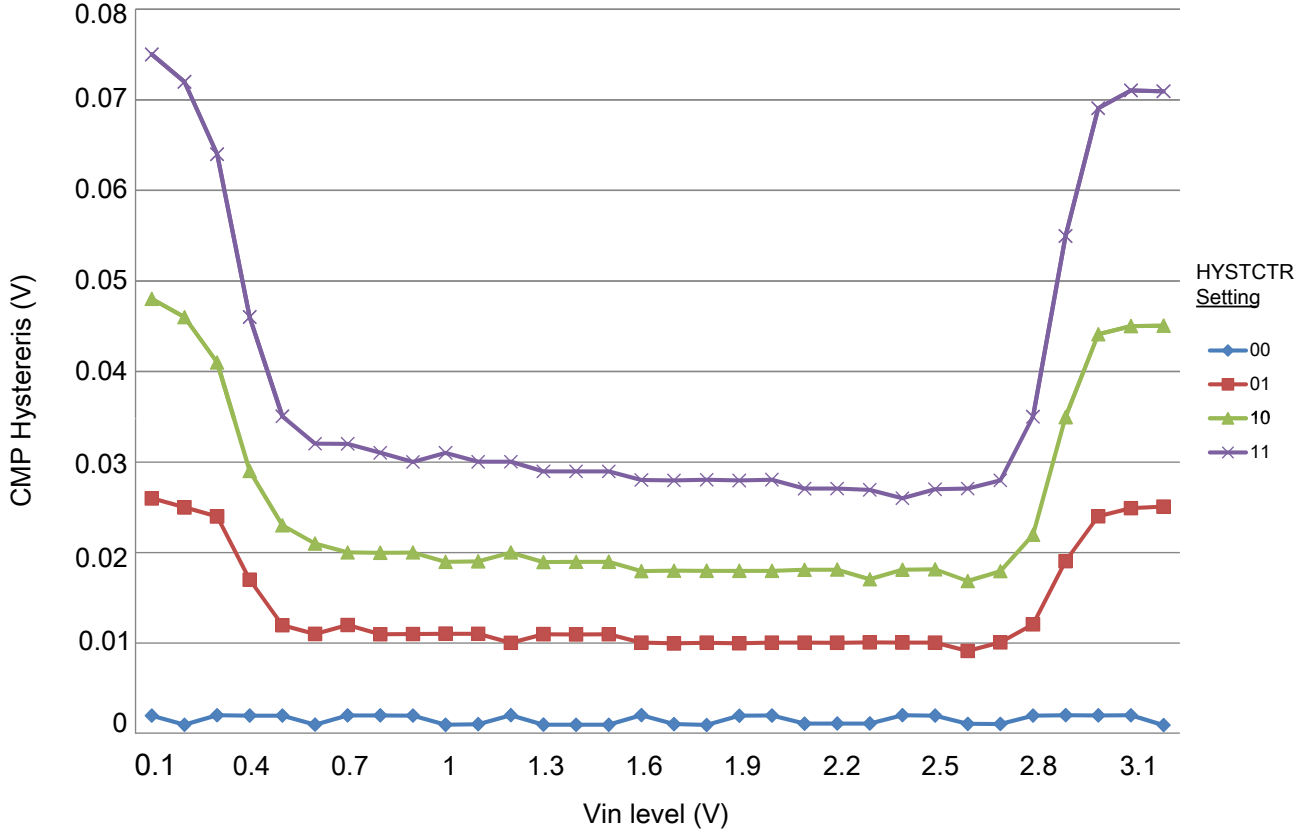
### 3.6.2 CMP and 6-bit DAC electrical specifications

**Table 28. Comparator and 6-bit DAC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply voltage	1.71	—	3.6	V
$I_{DDHS}$	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	$\mu$ A
$I_{DDL S}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	$\mu$ A
$V_{AIN}$	Analog input voltage	$V_{SS} - 0.3$	—	$V_{DD}$	V
$V_{AIO}$	Analog input offset voltage	—	—	20	mV
$V_H$	Analog comparator hysteresis <sup>1</sup> <ul style="list-style-type: none"> <li>• CR0[HYSTCTR] = 00</li> <li>• CR0[HYSTCTR] = 01</li> <li>• CR0[HYSTCTR] = 10</li> <li>• CR0[HYSTCTR] = 11</li> </ul>	—	5 10 20 30	—	mV
$V_{CMPOh}$	Output high	$V_{DD} - 0.5$	—	—	V
$V_{CMPOl}$	Output low	—	—	0.5	V
$t_{DHS}$	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
$t_{DLS}$	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay <sup>2</sup>	—	—	40	$\mu$ s
$I_{DAC6b}$	6-bit DAC current adder (enabled)	—	7	—	$\mu$ A
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB <sup>3</sup>
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

**Peripheral operating requirements and behaviors**

1. Typical hysteresis is measured with input voltage range limited to 0.6 to  $V_{DD}-0.6$  V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP\_DACCR[DACEN], CMP\_DACCR[VRSEL], CMP\_DACCR[VOSEL], CMP\_MUXCR[PSEL], and CMP\_MUXCR[MSEL]) and the comparator output settling to a stable level.
3.  $1 \text{ LSB} = V_{\text{reference}}/64$



**Figure 17. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)**



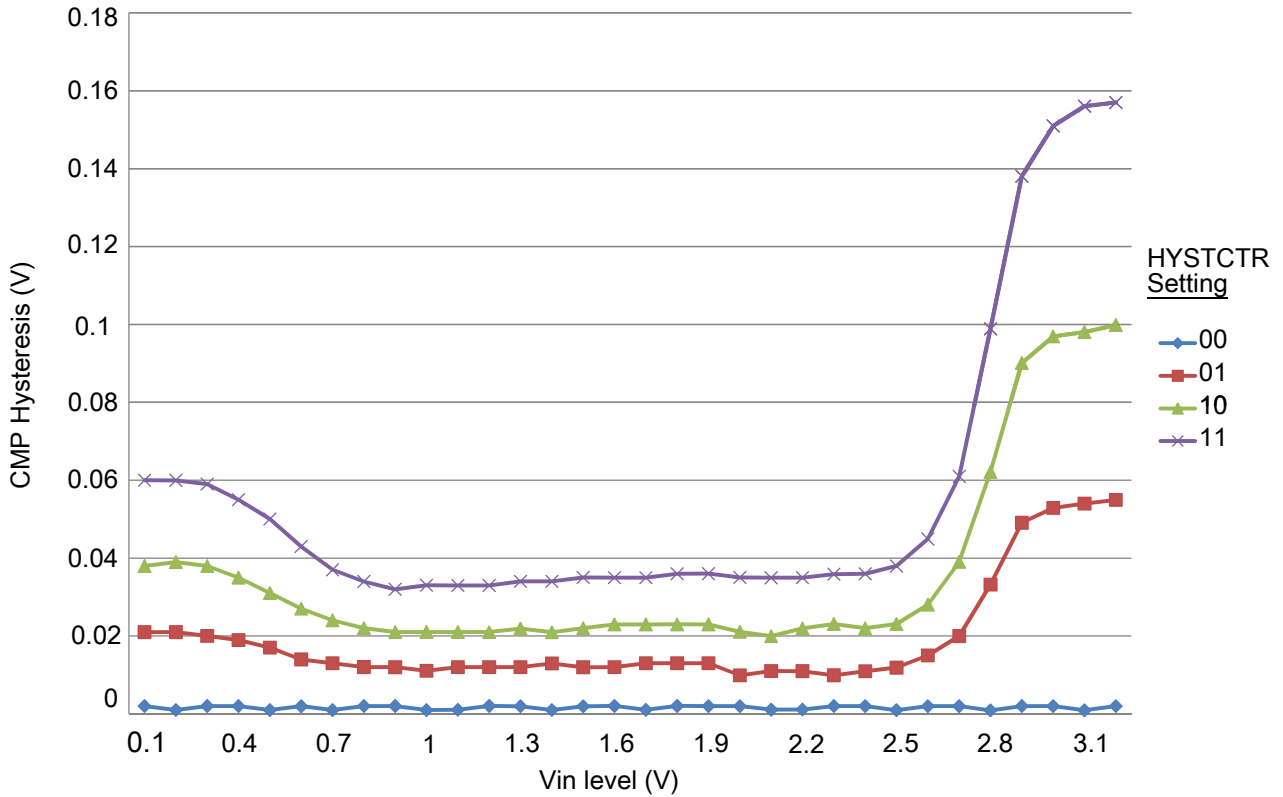


Figure 18. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

### 3.6.3 12-bit DAC electrical characteristics

#### 3.6.3.1 12-bit DAC operating requirements

Table 29. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	1.71	3.6	V	
$V_{DACR}$	Reference voltage	1.13	3.6	V	1
$C_L$	Output load capacitance	—	100	pF	2
$I_L$	Output load current	—	1	mA	

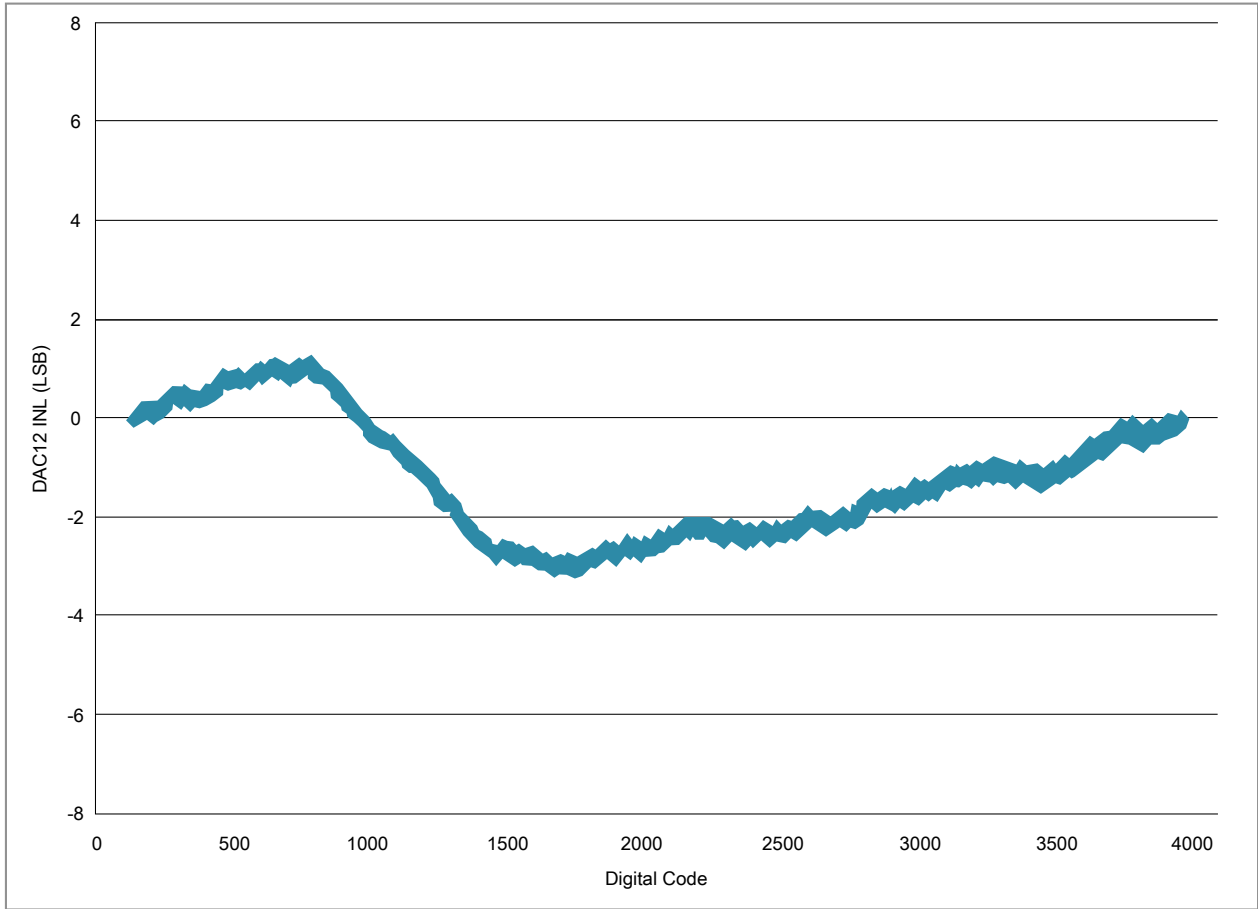
1. The DAC reference can be selected to be  $V_{DDA}$  or  $V_{REFH}$ .
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

### 3.6.3.2 12-bit DAC operating behaviors

Table 30. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA\_DACLP}$	Supply current — low-power mode	—	—	330	$\mu\text{A}$	
$I_{DDA\_DACHP}$	Supply current — high-speed mode	—	—	1200	$\mu\text{A}$	
$t_{DACLP}$	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	$\mu\text{s}$	1
$t_{DACHP}$	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	$\mu\text{s}$	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	$\mu\text{s}$	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFFF	$V_{DACR} - 100$	—	$V_{DACR}$	mV	
INL	Integral non-linearity error — high speed mode	—	—	$\pm 8$	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2\text{ V}$	—	—	$\pm 1$	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF\_OUT}$	—	—	$\pm 1$	LSB	4
$V_{OFFSET}$	Offset error	—	$\pm 0.4$	$\pm 0.8$	%FSR	5
$E_G$	Gain error	—	$\pm 0.1$	$\pm 0.6$	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4\text{ V}$	60	—	90	dB	
$T_{CO}$	Temperature coefficient offset voltage	—	3.7	—	$\mu\text{V}/\text{C}$	6
$T_{GE}$	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 k $\Omega$ )	—	—	250	$\Omega$	
SR	Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> <li>High power (SP<sub>HP</sub>)</li> <li>Low power (SP<sub>LP</sub>)</li> </ul>	1.2 0.05	1.7 0.12	— —	V/ $\mu\text{s}$	
BW	3dB bandwidth <ul style="list-style-type: none"> <li>High power (SP<sub>HP</sub>)</li> <li>Low power (SP<sub>LP</sub>)</li> </ul>	550 40	— —	— —	kHz	

- Settling within  $\pm 1$  LSB
- The INL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV with  $V_{DDA} > 2.4\text{ V}$
- Calculated by a best fit curve from  $V_{SS} + 100$  mV to  $V_{DACR} - 100$  mV
- $V_{DDA} = 3.0\text{ V}$ , reference select set for  $V_{DDA}$  (DACx\_CO:DACRFS = 1), high power mode (DACx\_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device



**Figure 19. Typical INL error vs. digital code**

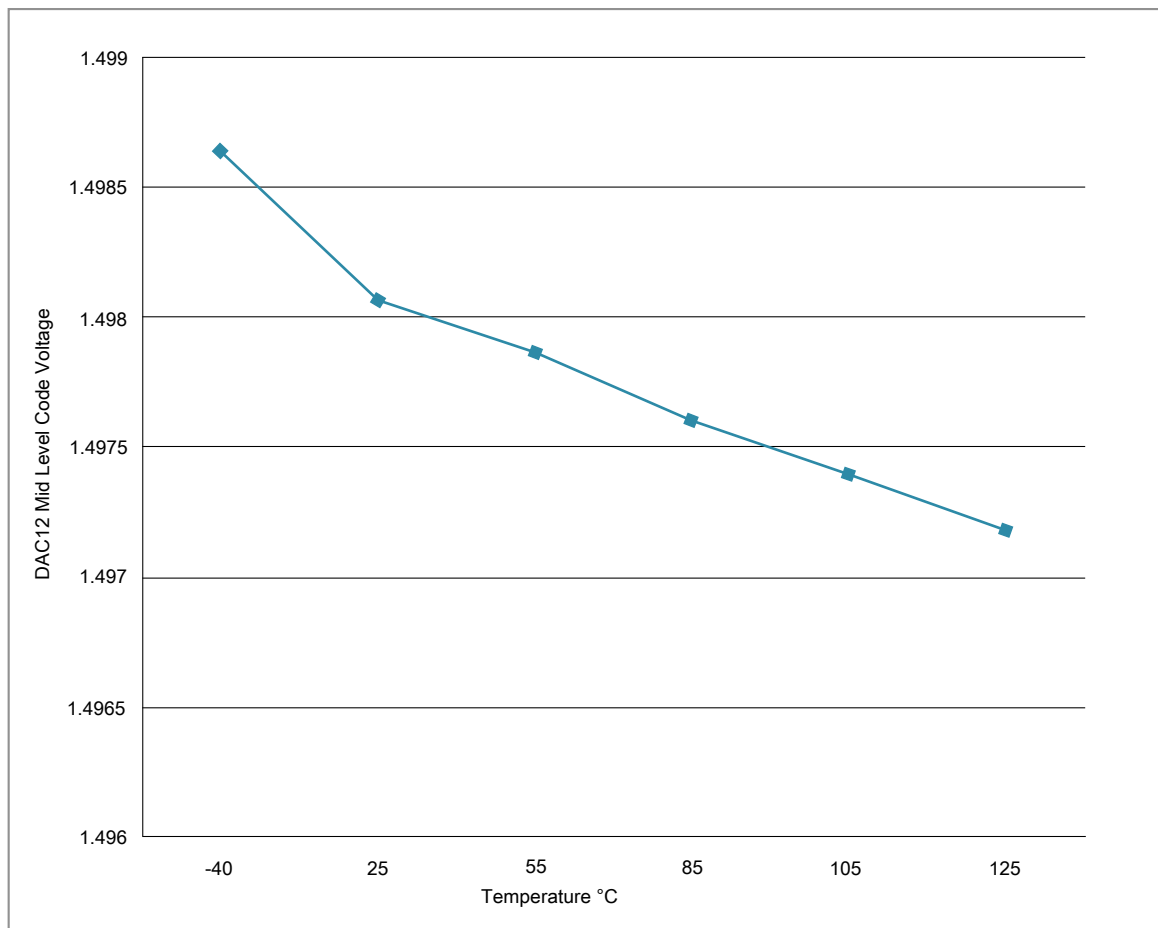


Figure 20. Offset at half scale vs. temperature

### 3.6.4 Voltage reference electrical specifications

Table 31. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>DDA</sub>	Supply voltage	1.71	3.6	V	
T <sub>A</sub>	Temperature	Operating temperature range of the device		°C	
C <sub>L</sub>	Output load capacitance	100		nF	1, 2

1. C<sub>L</sub> must be connected to VREF\_OUT if the VREF\_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C<sub>L</sub> value over the operating temperature range of the device.

**Table 32. VREF full-range operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{out}$	Voltage reference output with factory trim at nominal $V_{DDA}$ and temperature=25°C	1.1920	1.1950	1.1980	V	1
$V_{out}$	Voltage reference output with user trim at nominal $V_{DDA}$ and temperature=25°C	1.1945	1.1950	1.1955	V	1
$V_{step}$	Voltage reference trim step	—	0.5	—	mV	1
$V_{tdrift}$	Temperature drift ( $V_{max} - V_{min}$ across the full temperature range)	—	—	15	mV	1
$I_{bg}$	Bandgap only current	—	—	80	$\mu$ A	
$I_{lp}$	Low-power buffer current	—	—	360	$\mu$ A	1
$I_{hp}$	High-power buffer current	—	—	1	mA	1
$\Delta V_{LOAD}$	Load regulation • current = $\pm 1.0$ mA	—	200	—	$\mu$ V	1, 2
$T_{stup}$	Buffer startup time	—	—	100	$\mu$ s	
$T_{chop\_osc\_st\ up}$	Internal bandgap start-up delay with chop oscillator enabled	—	—	35	ms	
$V_{vdrift}$	Voltage drift ( $V_{max} - V_{min}$ across the full voltage range)	—	2	—	mV	1

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register.
2. Load regulation voltage is the difference between the VREF\_OUT voltage with no load vs. voltage with defined load

**Table 33. VREF limited-range operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$T_A$	Temperature	0	70	°C	

**Table 34. VREF limited-range operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{tdrift}$	Temperature drift ( $V_{max} - V_{min}$ across the limited temperature range)	—	10	mV	

## 3.7 Timers

See [General switching specifications](#).

## 3.8 Communication interfaces

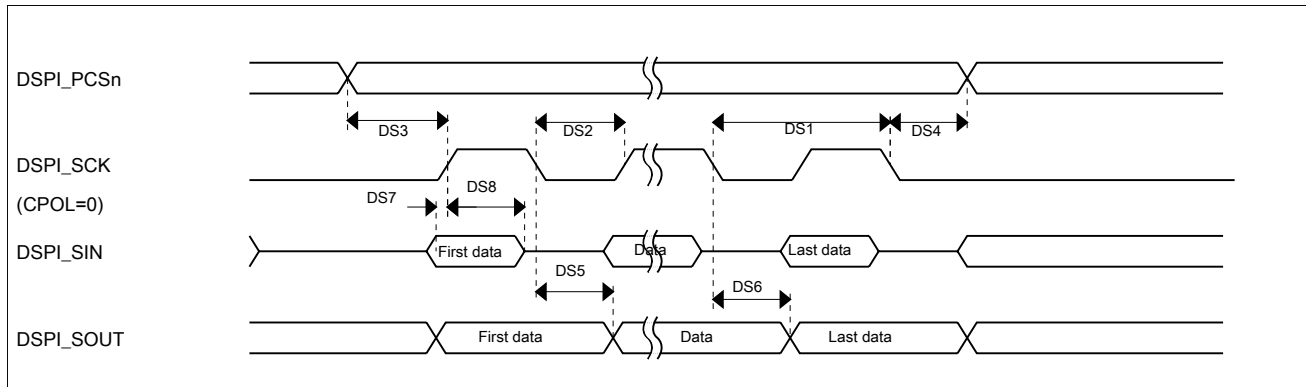
### 3.8.1 DSPI switching specifications (limited voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 35. Master mode DSPI timing (limited voltage range)**

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	30	MHz	
DS1	DSPI_SCK output cycle time	$2 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 2$	$(t_{SCK}/2) + 2$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	16.2	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx\_CTARn[PSSCK] and SPIx\_CTARn[CSSCK].
2. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].

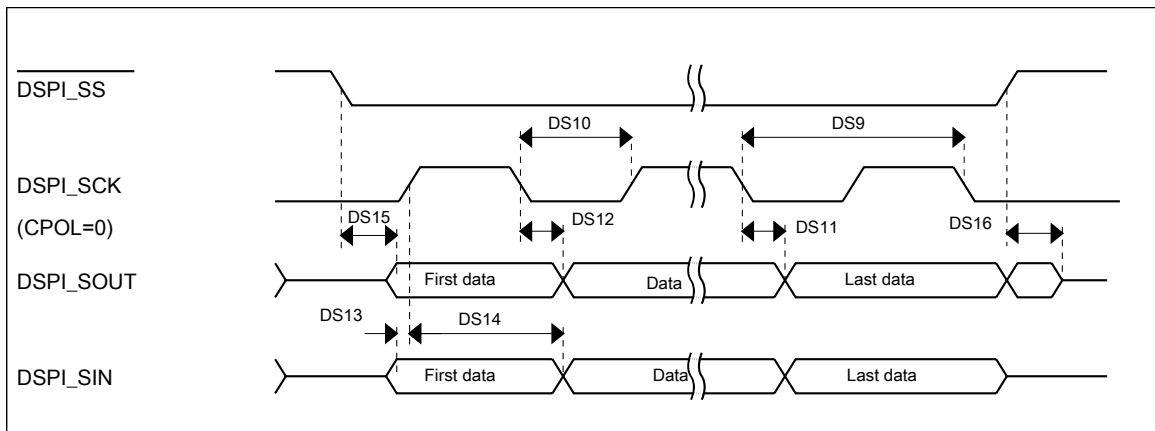


**Figure 21. DSPI classic SPI timing — master mode**

**Table 36. Slave mode DSPI timing (limited voltage range)**

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	2.7	3.6	V	
	Frequency of operation	—	15	MHz	1
DS9	DSPI_SCK input cycle time	$4 \times t_{\text{BUS}}$	—	ns	
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}}/2) - 2$	$(t_{\text{SCK}}/2) + 2$	ns	
DS11	DSPI_SCK to DSPI_SOUT valid	—	21.4	ns	
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns	
DS13	DSPI_SIN to DSPI_SCK input setup	2.6	—	ns	
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns	
DS15	DSPI_SS active to DSPI_SOUT driven	—	17	ns	
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	17	ns	

- The maximum operating frequency is measured with noncontinuous CS and SCK. When DSPI is configured with continuous CS and SCK, the SPI clock must not be greater than 1/6 of the bus clock. For example, when the bus clock is 60 MHz, the SPI clock must not be greater than 10 MHz.


**Figure 22. DSPI classic SPI timing — slave mode**

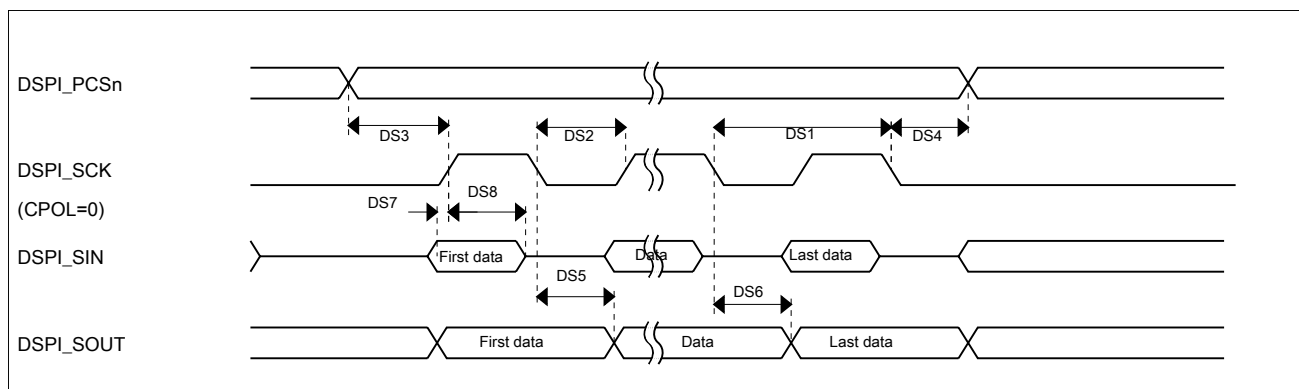
### 3.8.2 DSPI switching specifications (full voltage range)

The Deserial Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the SPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

**Table 37. Master mode DSPI timing (full voltage range)**

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	15	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK/2}) - 4$	$(t_{SCK/2}) + 4$	ns	
DS3	DSPI_PCSn valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24.6	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx\_CTARn[PSSCK] and SPIx\_CTARn[CSSCK].
3. The delay is programmable in SPIx\_CTARn[PASC] and SPIx\_CTARn[ASC].

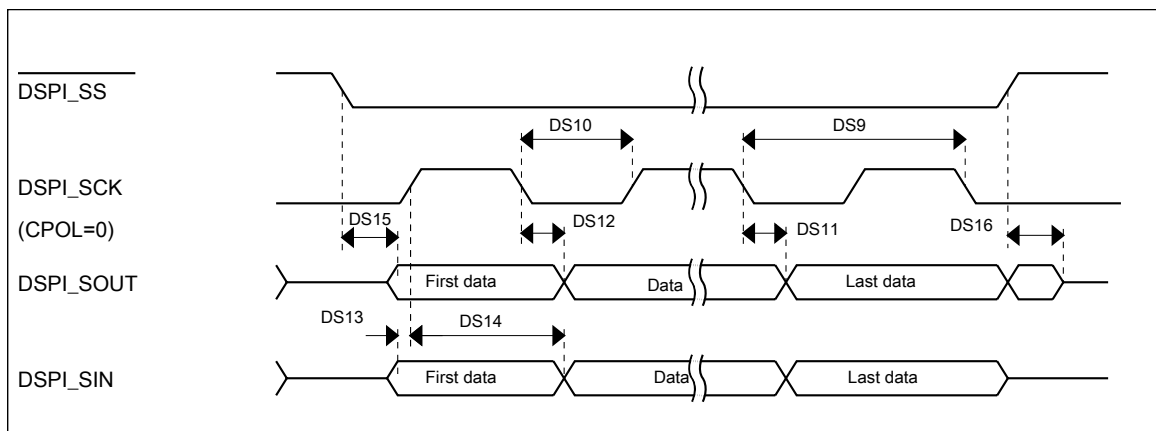


**Figure 23. DSPI classic SPI timing — master mode**



**Table 38. Slave mode DSPI timing (full voltage range)**

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	7.5	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{\text{BUS}}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}}/2) - 4$	$(t_{\text{SCK}}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	29.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	25	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	25	ns


**Figure 24. DSPI classic SPI timing — slave mode**

### 3.8.3 Inter-Integrated Circuit Interface (I<sup>2</sup>C) timing

**Table 39. I<sup>2</sup>C timing**

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	$f_{\text{SCL}}$	0	100	0	400 <sup>1</sup>	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{\text{HD}}$ ; STA	4	—	0.6	—	$\mu\text{s}$
LOW period of the SCL clock	$t_{\text{LOW}}$	4.7	—	1.25	—	$\mu\text{s}$
HIGH period of the SCL clock	$t_{\text{HIGH}}$	4	—	0.6	—	$\mu\text{s}$
Set-up time for a repeated START condition	$t_{\text{SU}}$ ; STA	4.7	—	0.6	—	$\mu\text{s}$

Table continues on the next page...

**Table 39. I<sup>2</sup>C timing (continued)**

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
Data hold time for I <sup>2</sup> C bus devices	t <sub>HD</sub> ; DAT	0 <sup>2</sup>	3.45 <sup>3</sup>	0 <sup>4</sup>	0.9 <sup>2</sup>	μs
Data set-up time	t <sub>SU</sub> ; DAT	250 <sup>5</sup>	—	100 <sup>3, 6</sup>	—	ns
Rise time of SDA and SCL signals	t <sub>r</sub>	—	1000	20 + 0.1C <sub>b</sub> <sup>7</sup>	300	ns
Fall time of SDA and SCL signals	t <sub>f</sub>	—	300	20 + 0.1C <sub>b</sub> <sup>6</sup>	300	ns
Set-up time for STOP condition	t <sub>SU</sub> ; STO	4	—	0.6	—	μs
Bus free time between STOP and START condition	t <sub>BUF</sub>	4.7	—	1.3	—	μs
Pulse width of spikes that must be suppressed by the input filter	t <sub>SP</sub>	N/A	N/A	0	50	ns

1. The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and VDD ≥ 2.7 V.
2. The master mode I<sup>2</sup>C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
3. The maximum t<sub>HD</sub>; DAT must be met only if the device does not stretch the LOW period (t<sub>LOW</sub>) of the SCL signal.
4. Input signal Slew = 10 ns and Output Load = 50 pF
5. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
6. A Fast mode I<sup>2</sup>C bus device can be used in a Standard mode I<sup>2</sup>C bus system, but the requirement t<sub>SU</sub>; DAT ≥ 250 ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line t<sub>rmax</sub> + t<sub>SU</sub>; DAT = 1000 + 250 = 1250 ns (according to the Standard mode I<sup>2</sup>C bus specification) before the SCL line is released.
7. C<sub>b</sub> = total capacitance of the one bus line in pF.

**Table 40. I<sup>2</sup>C 1 Mbps timing**

Characteristic	Symbol	Minimum	Maximum	Unit
SCL Clock Frequency	f <sub>SCL</sub>	0	1 <sup>1</sup>	MHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	t <sub>HD</sub> ; STA	0.26	—	μs
LOW period of the SCL clock	t <sub>LOW</sub>	0.5	—	μs
HIGH period of the SCL clock	t <sub>HIGH</sub>	0.26	—	μs
Set-up time for a repeated START condition	t <sub>SU</sub> ; STA	0.26	—	μs
Data hold time for I <sup>2</sup> C bus devices	t <sub>HD</sub> ; DAT	0	—	μs
Data set-up time	t <sub>SU</sub> ; DAT	50	—	ns
Rise time of SDA and SCL signals	t <sub>r</sub>	20 + 0.1C <sub>b</sub> <sup>2</sup>	120	ns
Fall time of SDA and SCL signals	t <sub>f</sub>	20 + 0.1C <sub>b</sub> <sup>2</sup>	120	ns
Set-up time for STOP condition	t <sub>SU</sub> ; STO	0.26	—	μs
Bus free time between STOP and START condition	t <sub>BUF</sub>	0.5	—	μs
Pulse width of spikes that must be suppressed by the input filter	t <sub>SP</sub>	0	50	ns

1. The maximum SCL clock frequency of 1 Mbps can support maximum bus loading when using the High drive pins across the full voltage range.
2. C<sub>b</sub> = total capacitance of the one bus line in pF.

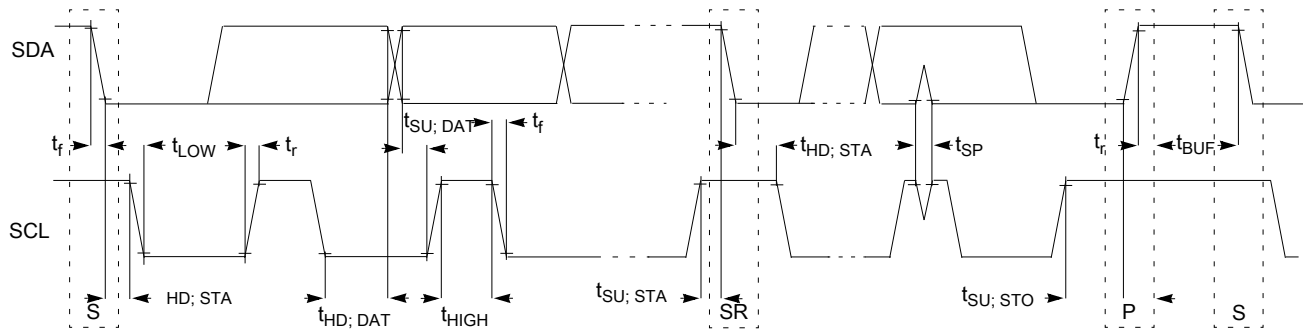


Figure 25. Timing definition for devices on the I<sup>2</sup>C bus

### 3.8.4 UART switching specifications

See [General switching specifications](#).

## 3.9 Kinetis Motor Suite

Kinetis Motor Suite is a bundled software solution that enables the rapid configuration of motor drive systems, and accelerates development of the final motor drive application.

Several members of the KV3x family are enabled with Kinetis motor suite. The enabled devices can be identified within the orderable part numbers in [this table](#). For more information refer to Kinetis Motor Suite User's Guide (KMS100UG) and Kinetis Motor Suite API Reference Manual (KMS100RM).

### NOTE

To find the associated resource, go to [freescale.com](http://freescale.com) and perform a search using Document ID.

## 4 Dimensions

### 4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to [freescale.com](http://freescale.com) and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
64-pin LQFP	<a href="#">98ASS23234W</a>
100-pin LQFP	<a href="#">98ASS23308W</a>

## 5 Pinout

### 5.1 KV31F Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	1	PTE0/ CLKOUT32K	ADC1_SE4a	ADC1_SE4a	PTE0/ CLKOUT32K	SPI1_PCS1	UART1_TX			I2C1_SDA		
2	2	PTE1/ LLWU_P0	ADC1_SE5a	ADC1_SE5a	PTE1/ LLWU_P0	SPI1_SOUT	UART1_RX			I2C1_SCL	SPI1_SIN	
3	—	PTE2/ LLWU_P1	ADC1_SE6a	ADC1_SE6a	PTE2/ LLWU_P1	SPI1_SCK	UART1_ CTS_b					
4	—	PTE3	ADC1_SE7a	ADC1_SE7a	PTE3	SPI1_SIN	UART1_ RTS_b				SPI1_SOUT	
5	—	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2	SPI1_PCS0	LPUART0_ TX					
6	—	PTE5	DISABLED		PTE5	SPI1_PCS2	LPUART0_ RX			FTM3_CH0		
7	—	PTE6	DISABLED		PTE6	SPI1_PCS3	LPUART0_ CTS_b			FTM3_CH1		
8	3	VDD	VDD	VDD								
9	4	VSS	VSS	VSS								
10	5	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
11	6	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPTMR0_ ALT3		
12	7	PTE18	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_ CTS_b	I2C0_SDA				
13	8	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_ RTS_b	I2C0_SCL				
14	—	ADC0_DP1	ADC0_DP1	ADC0_DP1								
15	—	ADC0_DM1	ADC0_DM1	ADC0_DM1								
16	—	ADC1_DP1/ ADC0_DP2	ADC1_DP1/ ADC0_DP2	ADC1_DP1/ ADC0_DP2								

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
17	—	ADC1_DM1/ ADC0_DM2	ADC1_DM1/ ADC0_DM2	ADC1_DM1/ ADC0_DM2								
18	9	ADC0_DP0/ ADC1_DP3	ADC0_DP0/ ADC1_DP3	ADC0_DP0/ ADC1_DP3								
19	10	ADC0_DM0/ ADC1_DM3	ADC0_DM0/ ADC1_DM3	ADC0_DM0/ ADC1_DM3								
20	11	ADC1_DP0/ ADC0_DP3	ADC1_DP0/ ADC0_DP3	ADC1_DP0/ ADC0_DP3								
21	12	ADC1_DM0/ ADC0_DM3	ADC1_DM0/ ADC0_DM3	ADC1_DM0/ ADC0_DM3								
22	13	VDDA	VDDA	VDDA								
23	14	VREFH	VREFH	VREFH								
24	15	VREFL	VREFL	VREFL								
25	16	VSSA	VSSA	VSSA								
26	17	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
27	18	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23	DAC0_OUT/ CMP1_IN3/ ADC0_SE23								
28	19	DAC1_OUT/ CMP0_IN4/ ADC1_SE23	DAC1_OUT/ CMP0_IN4/ ADC1_SE23	DAC1_OUT/ CMP0_IN4/ ADC1_SE23								
29	—	VSS	VSS	VSS								
30	—	VDD	VDD	VDD								
31	20	PTE24	ADC0_SE17	ADC0_SE17	PTE24		FTM0_CH0		I2C0_SCL	EWM_OUT_ b		
32	21	PTE25	ADC0_SE18	ADC0_SE18	PTE25		FTM0_CH1		I2C0_SDA	EWM_IN		
33	—	PTE26/ CLKOUT32K	DISABLED		PTE26/ CLKOUT32K							
34	22	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK		PTA0	UART0_ CTS_b	FTM0_CH5		EWM_IN		JTAG_TCLK/ SWD_CLK	EZP_CLK
35	23	PTA1	JTAG_TDI/ EZP_DI		PTA1	UART0_RX	FTM0_CH6	CMP0_OUT	FTM2_QD_ PHA	FTM1_CH1	JTAG_TDI	EZP_DI
36	24	PTA2	JTAG_TDO/ TRACE_ SWO/ EZP_DO		PTA2	UART0_TX	FTM0_CH7	CMP1_OUT	FTM2_QD_ PHB	FTM1_CH0	JTAG_TDO/ TRACE_ SWO	EZP_DO
37	25	PTA3	JTAG_TMS/ SWD_DIO		PTA3	UART0_ RTS_b	FTM0_CH0	FTM2_FLT0	EWM_OUT_ b		JTAG_TMS/ SWD_DIO	
38	26	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b		PTA4/ LLWU_P3		FTM0_CH1		FTM0_FLT3		NMI_b	EZP_CS_b
39	27	PTA5	DISABLED		PTA5		FTM0_CH2				JTAG_ TRST_b	



## Pinout

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
40	—	VDD	VDD	VDD								
41	—	VSS	VSS	VSS								
42	28	PTA12	DISABLED		PTA12		FTM1_CH0				FTM1_QD_PHA	
43	29	PTA13/LLWU_P4	DISABLED		PTA13/LLWU_P4		FTM1_CH1				FTM1_QD_PHB	
44	—	PTA14	DISABLED		PTA14	SPI0_PCS0	UART0_TX					
45	—	PTA15	DISABLED		PTA15	SPI0_SCK	UART0_RX					
46	—	PTA16	DISABLED		PTA16	SPI0_SOUT	UART0_CTS_b					
47	—	PTA17	ADC1_SE17	ADC1_SE17	PTA17	SPI0_SIN	UART0_RTS_b					
48	30	VDD	VDD	VDD								
49	31	VSS	VSS	VSS								
50	32	PTA18	EXTAL0	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
51	33	PTA19	XTAL0	XTAL0	PTA19	FTM0_FLT0	FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
52	34	RESET_b	RESET_b	RESET_b								
53	35	PTB0/LLWU_P5	ADC0_SE8/ADC1_SE8	ADC0_SE8/ADC1_SE8	PTB0/LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_PHA	UART0_RX	
54	36	PTB1	ADC0_SE9/ADC1_SE9	ADC0_SE9/ADC1_SE9	PTB1	I2C0_SDA	FTM1_CH1	FTM0_FLT2	EWM_IN	FTM1_QD_PHB	UART0_TX	
55	37	PTB2	ADC0_SE12	ADC0_SE12	PTB2	I2C0_SCL	UART0_RTS_b	FTM0_FLT1		FTM0_FLT3		
56	38	PTB3	ADC0_SE13	ADC0_SE13	PTB3	I2C0_SDA	UART0_CTS_b			FTM0_FLT0		
57	—	PTB9	DISABLED		PTB9	SPI1_PCS1	LPUART0_CTS_b		FB_AD20			
58	—	PTB10	ADC1_SE14	ADC1_SE14	PTB10	SPI1_PCS0	LPUART0_RX		FB_AD19	FTM0_FLT1		
59	—	PTB11	ADC1_SE15	ADC1_SE15	PTB11	SPI1_SCK	LPUART0_TX		FB_AD18	FTM0_FLT2		
60	—	VSS	VSS	VSS								
61	—	VDD	VDD	VDD								
62	39	PTB16	DISABLED		PTB16	SPI1_SOUT	UART0_RX	FTM_CLKIN0	FB_AD17	EWM_IN		
63	40	PTB17	DISABLED		PTB17	SPI1_SIN	UART0_TX	FTM_CLKIN1	FB_AD16	EWM_OUT_b		
64	41	PTB18	DISABLED		PTB18		FTM2_CH0		FB_AD15	FTM2_QD_PHA		
65	42	PTB19	DISABLED		PTB19		FTM2_CH1		FB_OE_b	FTM2_QD_PHB		
66	—	PTB20	DISABLED		PTB20				FB_AD31	CMP0_OUT		
67	—	PTB21	DISABLED		PTB21				FB_AD30	CMP1_OUT		
68	—	PTB22	DISABLED		PTB22				FB_AD29			

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
69	—	PTB23	DISABLED		PTB23		SPI0_PCS5		FB_AD28			
70	43	PTC0	ADC0_SE14	ADC0_SE14	PTC0	SPI0_PCS4	PDB0_EXTRG		FB_AD14	FTM0_FLT1	SPI0_PCS0	
71	44	PTC1/LLWU_P6	ADC0_SE15	ADC0_SE15	PTC1/LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FB_AD13		LPUART0_RTS_b	
72	45	PTC2	ADC0_SE4b/CMP1_IN0	ADC0_SE4b/CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FB_AD12		LPUART0_CTS_b	
73	46	PTC3/LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT		LPUART0_RX	
74	47	VSS	VSS	VSS								
75	48	VDD	VDD	VDD								
76	49	PTC4/LLWU_P8	DISABLED		PTC4/LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3	FB_AD11	CMP1_OUT	LPUART0_TX	
77	50	PTC5/LLWU_P9	DISABLED		PTC5/LLWU_P9	SPI0_SCK	LPTMR0_ALT2		FB_AD10	CMP0_OUT	FTM0_CH2	
78	51	PTC6/LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/LLWU_P10	SPI0_SOUT	PDB0_EXTRG		FB_AD9		I2C0_SCL	
79	52	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN			FB_AD8		I2C0_SDA	
80	53	PTC8	ADC1_SE4b/CMP0_IN2	ADC1_SE4b/CMP0_IN2	PTC8		FTM3_CH4		FB_AD7			
81	54	PTC9	ADC1_SE5b/CMP0_IN3	ADC1_SE5b/CMP0_IN3	PTC9		FTM3_CH5		FB_AD6	FTM2_FLT0		
82	55	PTC10	ADC1_SE6b	ADC1_SE6b	PTC10	I2C1_SCL	FTM3_CH6		FB_AD5			
83	56	PTC11/LLWU_P11	ADC1_SE7b	ADC1_SE7b	PTC11/LLWU_P11	I2C1_SDA	FTM3_CH7		FB_RW_b			
84	—	PTC12	DISABLED		PTC12				FB_AD27	FTM3_FLT0		
85	—	PTC13	DISABLED		PTC13				FB_AD26			
86	—	PTC14	DISABLED		PTC14				FB_AD25			
87	—	PTC15	DISABLED		PTC15				FB_AD24			
88	—	VSS	VSS	VSS								
89	—	VDD	VDD	VDD								
90	—	PTC16	DISABLED		PTC16		LPUART0_RX		FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_BLS15_8_b			
91	—	PTC17	DISABLED		PTC17		LPUART0_TX		FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_BLS7_0_b			
92	—	PTC18	DISABLED		PTC18		LPUART0_RTS_b		FB_TBST_b/ FB_CS2_b/ FB_BE15_8_BLS23_16_b			

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
93	57	PTD0/LLWU_P12	DISABLED		PTD0/LLWU_P12	SPI0_PCS0	UART2_RTS_b	FTM3_CH0	FB_ALE/ FB_CS1_b/ FB_TS_b	LPUART0_RTS_b		
94	58	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_b	FTM3_CH1	FB_CS0_b	LPUART0_CTS_b		
95	59	PTD2/LLWU_P13	DISABLED		PTD2/LLWU_P13	SPI0_SOUT	UART2_RX	FTM3_CH2	FB_AD4	LPUART0_RX	I2C0_SCL	
96	60	PTD3	DISABLED		PTD3	SPI0_SIN	UART2_TX	FTM3_CH3	FB_AD3	LPUART0_TX	I2C0_SDA	
97	61	PTD4/LLWU_P14	DISABLED		PTD4/LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4	FB_AD2	EWM_IN	SPI1_PCS0	
98	62	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_b	FTM0_CH5	FB_AD1	EWM_OUT_b	SPI1_SCK	
99	63	PTD6/LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FB_AD0	FTM0_FLT0	SPI1_SOUT	
100	64	PTD7	DISABLED		PTD7		UART0_TX	FTM0_CH7		FTM0_FLT1	SPI1_SIN	

## 5.2 Recommended connection for unused analog and digital pins

The following table shows the recommended connections for analog interface pins if those analog interfaces are not used in the customer's application.

**Table 41. Recommended connection for unused analog interfaces**

Pin Type		Short recommendation	Detailed recommendation
Analog/non GPIO	PGAx/ADCx	Float	Analog input - Float
Analog/non GPIO	ADCx/CMPx	Float	Analog input - Float
Analog/non GPIO	VREF_OUT	Float	Analog output - Float
Analog/non GPIO	DACx_OUT	Float	Analog output - Float
Analog/non GPIO	RTC_WAKEUP_B	Float	Analog output - Float
Analog/non GPIO	XTAL32	Float	Analog output - Float
Analog/non GPIO	EXTAL32	Float	Analog input - Float
GPIO/Analog	PTA18/EXTAL0	Float	Analog input - Float
GPIO/Analog	PTA19/XTAL0	Float	Analog output - Float
GPIO/Analog	PTx/ADCx	Float	Float (default is analog input)
GPIO/Analog	PTx/CMPx	Float	Float (default is analog input)
GPIO/Digital	PTA0/JTAG_TCLK	Float	Float (default is JTAG with pulldown)
GPIO/Digital	PTA1/JTAG_TDI	Float	Float (default is JTAG with pullup)

Table continues on the next page...



**Table 41. Recommended connection for unused analog interfaces (continued)**

Pin Type		Short recommendation	Detailed recommendation
GPIO/Digital	PTA2/JTAG_TDO	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA3/JTAG_TMS	Float	Float (default is JTAG with pullup)
GPIO/Digital	PTA4/NMI_b	10kΩ pullup or disable and float	Pull high or disable in PCR & FOPT and float
GPIO/Digital	PTx	Float	Float (default is disabled)
VDDA	VDDA	Always connect to VDD potential	Always connect to VDD potential
VREFH	VREFH	Always connect to VDD potential	Always connect to VDD potential
VREFL	VREFL	Always connect to VSS potential	Always connect to VSS potential
VSSA	VSSA	Always connect to VSS potential	Always connect to VSS potential

### 5.3 KV31F Pinouts

The following figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

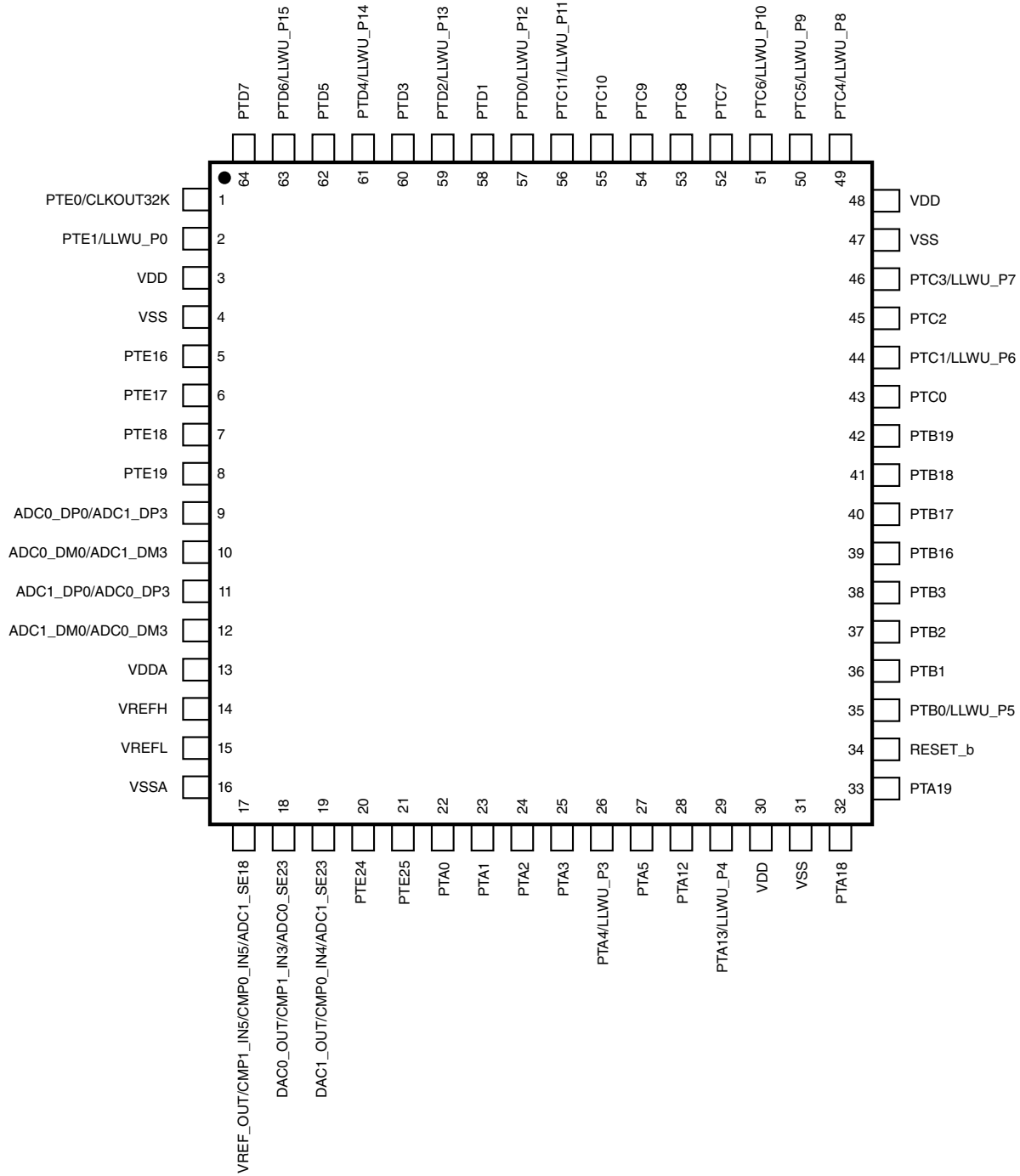


Figure 26. KV31F 64 LQFP Pinout Diagram (top view)



## 6.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 6.2 Format

Part numbers for this device have the following format:

Q KV## A FFF R T PP CC S N

## 6.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
KV##	Kinetis V Series	<ul style="list-style-type: none"> <li>KV3x: Cortex-M4 based MCU</li> </ul>
A	Key attribute	<ul style="list-style-type: none"> <li>D = Cortex-M4 w/ DSP</li> <li>F = Cortex-M4 w/ DSP and FPU</li> </ul>
FFF	Program flash memory size	<ul style="list-style-type: none"> <li>64 = 64 KB</li> <li>128 = 128 KB</li> <li>256 = 256 KB</li> <li>512 = 512 KB</li> </ul>
R	Silicon revision	<ul style="list-style-type: none"> <li>(Blank) = Main</li> <li>A = Revision after main</li> </ul>
T	Temperature range (°C)	<ul style="list-style-type: none"> <li>V = -40 to 105</li> <li>C = -40 to 85</li> </ul>
PP	Package identifier	<ul style="list-style-type: none"> <li>FM = 32 QFN (5 mm x 5 mm)</li> <li>LF = 48 LQFP (7 mm x 7 mm)</li> <li>LH = 64 LQFP (10 mm x 10 mm)</li> <li>LL = 100 LQFP (14 mm x 14 mm)</li> <li>MC = 121 XFBGA (8 mm x 8 mm)</li> <li>DC = 121 XFBGA (8 mm x 8 mm x 0.5 mm)</li> </ul>
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"> <li>10 = 100 MHz</li> <li>12 = 120 MHz</li> </ul>
S	Software type	<ul style="list-style-type: none"> <li>P = KMS-PMSM and BLDC</li> <li>(Blank) = Not software enabled</li> </ul>
N	Packaging type	<ul style="list-style-type: none"> <li>R = Tape and reel</li> <li>(Blank) = Trays</li> </ul>

## 6.4 Example

This is an example part number:

MKV31F512VLL12P

# 7 Terminology and guidelines

## 7.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	<p>A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:</p> <ul style="list-style-type: none"> <li>• <i>Operating ratings</i> apply during operation of the chip.</li> <li>• <i>Handling ratings</i> apply when the chip is not powered.</li> </ul> <p><b>NOTE:</b> The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.</p>
Operating requirement	<p>A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip</p>
Operating behavior	<p>A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions</p>
Typical value	<p>A specified value for a technical characteristic that:</p> <ul style="list-style-type: none"> <li>• Lies within the range of values specified by the operating behavior</li> <li>• Is representative of that characteristic during operation when you meet the <a href="#">typical-value conditions</a> or other specified conditions</li> </ul> <p><b>NOTE:</b> Typical values are provided as design guidelines and are neither tested nor guaranteed.</p>

## 7.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	-0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a typical value:

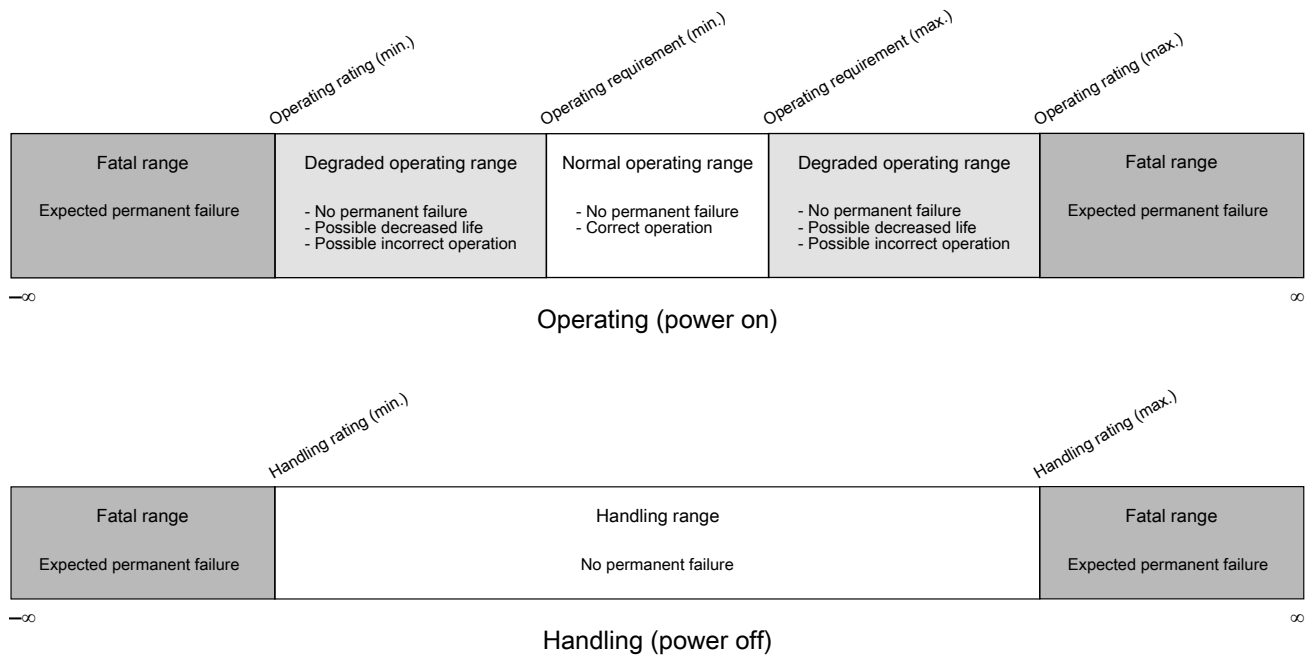
Symbol	Description	Min.	Typ.	Max.	Unit
I <sub>WP</sub>	Digital I/O weak pullup/pulldown current	10	70	130	μA

## 7.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T <sub>A</sub>	Ambient temperature	25	°C
V <sub>DD</sub>	Supply voltage	3.3	V

## 7.4 Relationship between ratings and operating requirements



## 7.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

## 8 Revision History

The following table provides a revision history for this document.

**Table 42. Revision History**

Rev. No.	Date	Substantial Changes
7	02/2016	<ul style="list-style-type: none"> <li>• Added KMS related information in front matter</li> <li>• Added Kinetis Motor Suite section</li> <li>• Added "S" in Format and Part Identification table</li> <li>• Updated the Part Number Example</li> </ul>

*Table continues on the next page...*

**Table 42. Revision History (continued)**

Rev. No.	Date	Substantial Changes
		<ul style="list-style-type: none"> <li>Added Terminology and Guidelines section</li> <li>Updated IRC48M specifications table</li> </ul>
6	10/2015	<ul style="list-style-type: none"> <li>In "Power consumption operating behaviors" section, added "Low power mode peripheral adders—typical value" table</li> <li>In "Thermal operating requirements" table, in footnote, corrected "<math>T_J = T_A + \Theta_{JA}</math>" to "<math>T_J = T_A + R_{\Theta JA}</math>"</li> <li>Updated "IRC48M specifications" table</li> <li>Updated "NVM program/erase timing specifications" table; removed row for <math>t_{hversall}</math> and added row for <math>t_{hversblk256k}</math></li> <li>Updated "Flash command timing specifications" table; added rows for <math>t_{rd1blk256k}</math> and <math>t_{ersblk256k}</math></li> <li>In "Slave mode DSPI timing (limited voltage range)" table, added footnote regarding maximum frequency of operation</li> <li>Added new section, "Recommended connections for unused analog and digital pins"</li> </ul>
5	4/2015	<ul style="list-style-type: none"> <li>On page 1:               <ul style="list-style-type: none"> <li>Under "Security and integrity modules" added "Hardware random-number generator"</li> <li>Under "Communication interfaces," updated I<sup>2</sup>C bullet to indicate support for up to 1 Mbps operation</li> <li>Under "Operating characteristics," specified that voltage range includes flash writes</li> </ul> </li> <li>In figure, "Functional block diagram," added "Random-number generator."</li> <li>In "Voltage and current operating requirements" table:               <ul style="list-style-type: none"> <li>Removed content related to positive injection</li> <li>Updated footnote 1 to say that all analog and I/O pins are internally clamped to V<sub>SS</sub> only (not V<sub>SS</sub> and V<sub>DD</sub>) through ESD protection diodes.</li> </ul> </li> <li>In "Power consumption operating behaviors" table:               <ul style="list-style-type: none"> <li>Added additional temperature data in power consumption table</li> <li>Added Max IDD values based on characterization results equivalent to mean + 3 sigma</li> </ul> </li> <li>Updated "EMC radiated emissions operating behaviors" table</li> <li>In "Thermal operating requirements" table, added the following footnote for ambient temperature: "Maximum T<sub>A</sub> can be exceeded only if the user ensures that T<sub>J</sub> does not exceed maximum T<sub>J</sub>. The simplest method to determine T<sub>J</sub> is: <math>T_J = T_A + \Theta_{JA} \times</math> chip power dissipation"</li> <li>Updated "IRC48M Specifications":               <ul style="list-style-type: none"> <li>Updated maximum values for <math>\Delta_{firc48m\_lv}</math> and <math>\Delta_{firc48m\_hv}</math> (full temperature)</li> <li>Added specifications for <math>\Delta_{firc48m\_hv}</math> (-40°C to 85°C)</li> </ul> </li> <li>In "I<sup>2</sup>C timing" table,               <ul style="list-style-type: none"> <li>Added the following footnote on maximum Fast mode value for SCL Clock Frequency: "The maximum SCL Clock Frequency in Fast mode with maximum bus loading can only be achieved when using the High drive pins across the full voltage range and when using the Normal drive pins and VDD ≥ 2.7 V."</li> <li>Updated minimum Fast mode value for LOW period of the SCL clock to 1.25 μ</li> </ul> </li> <li>Added "I<sup>2</sup>C 1 Mbps timing" table</li> <li>Removed Section 6, "Ordering parts."</li> <li>Specified that the figure, "KV31F 64 LQFP Pinout Diagram" is a top view</li> <li>Specified that the figure, "KV31F 100 LQFP Pinout Diagram" is a top view</li> </ul>
4	7/2014	<ul style="list-style-type: none"> <li>In "Power consumption operating behaviors table":</li> </ul>

*Table continues on the next page...*



**Table 42. Revision History (continued)**

Rev. No.	Date	Substantial Changes
		<ul style="list-style-type: none"> <li>• Updated existing typical power measurements</li> <li>• Added new typical power measurements for the following:               <ul style="list-style-type: none"> <li>• IDD_HSRUN (High Speed Run mode current executing CoreMark code)</li> <li>• IDD_RUNCO (Run mode current in Compute operation, executing CoreMark code)</li> <li>• IDD_RUN (Run mode current in Compute operation, executing while(1) loop)</li> <li>• IDD_VLPR (Very Low Power mode current executing CoreMark code)</li> <li>• IDD_VLPR (Very Low Power Run mode current in Compute operation, executing while(1) loop)</li> </ul> </li> </ul>
3	5/2014	<ul style="list-style-type: none"> <li>• In "Voltage and current operating ratings" table, updated maximum digital supply current</li> <li>• Updated "Voltage and current operating behaviors" table</li> <li>• Updated "Power mode transition operating behaviors" table</li> <li>• Updated "Power consumption operating behaviors" table</li> <li>• Updated "EMC radiated emissions operating behaviors for 64 LQFP package" table</li> <li>• Updated "Thermal attributes" table</li> <li>• Updated "MCG specifications" table</li> <li>• Updated "IRC48M specifications" table</li> <li>• Updated "16-bit ADC operating conditions" table</li> <li>• Updated "Voltage reference electrical specifications" section</li> </ul>
2	3/2014	Initial public release



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Document Number KV31P100M120SF7  
Revision 7, 02/2016

